

1	Cover Sheet
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3	Clock Distribution
4	CPU-CLK/Control/MISC/PEG
5	CPU-Memory
6	CPU-Power
7	CPU-GND
8	DDR III DIMM 1/DIMM 2
9	PCH-PCIE/DMI/USB/CLK
10	PCH-SATA/HOST/GPIO/DDI/VGA
11	PCH-SMB/LPC/AUDIO/RTC
12	PCH-Power
13	PCH-GND
14	SIO-NCT6779D
15	PCIE x16 & x1 Slots
16	PCIE To PCI Bridge
17	PCI Slot
18	LAN-RTL8111GN/RTL8111E-VC
19	Audio-ALC662VD
20	Front/Rear USB Connectors
21	SATA/FAN
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27	VCCP
28	ATX/F_Panel/EMI/LED
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33	Reset/Pwrok/PON
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IH81M

Version : 0E

CPU :

Intel Haswell Processor

System Chipset :

Intel Lynx Point Chipset

On Board Chipset :

VRM 12.5 -- NCP81102+NCP81161 4Phase

Gigabit LAN -- RTL8111GN Co-lay RTL8111E-VC

HDA Codec -- Realtek ALC662VD

Super I/O -- NCT6779D

SPI Flash 64Mb

Main Memory :

2 Channel DDR III * 2 (Max 16GB)

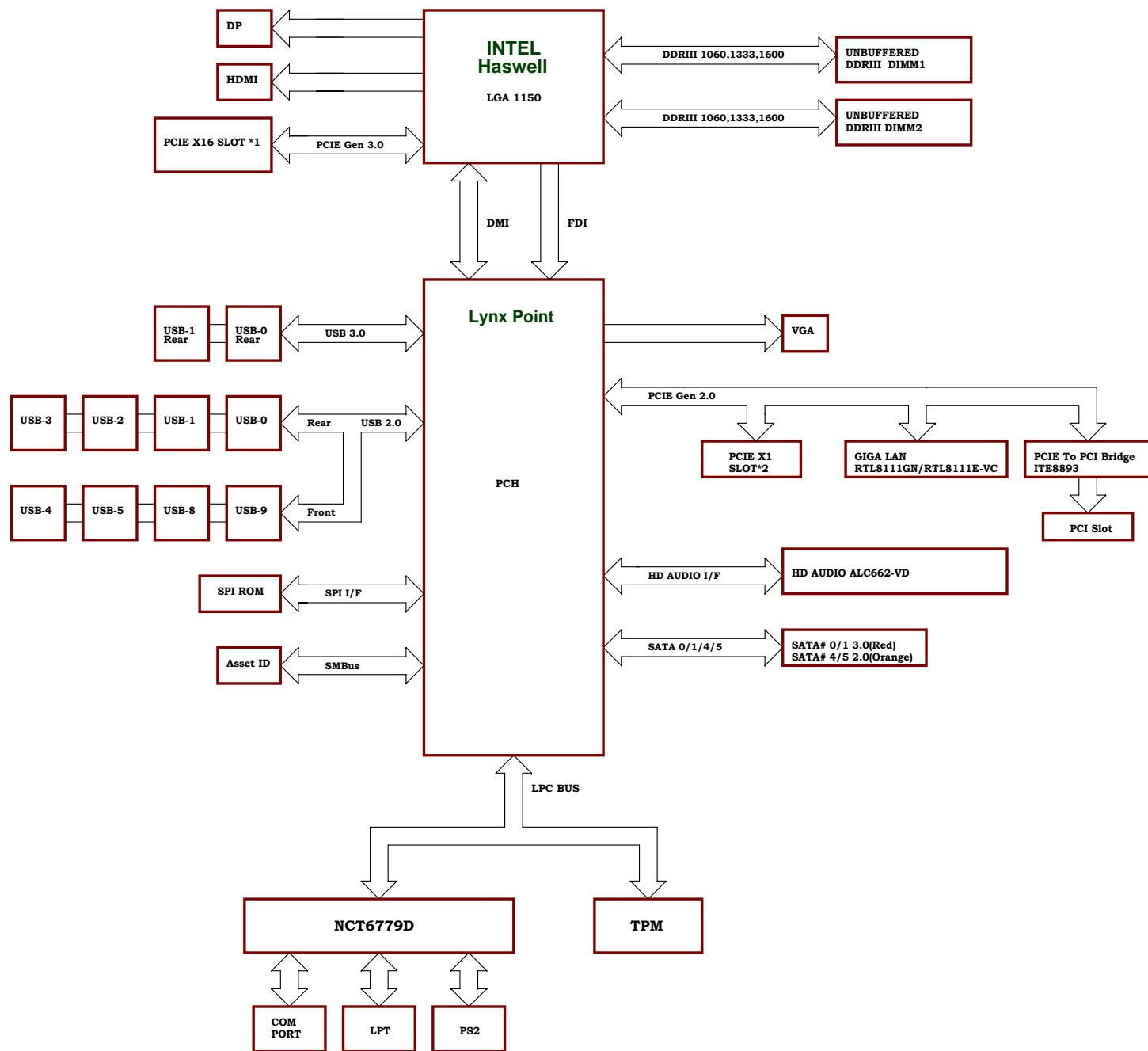
Expansion Slot :

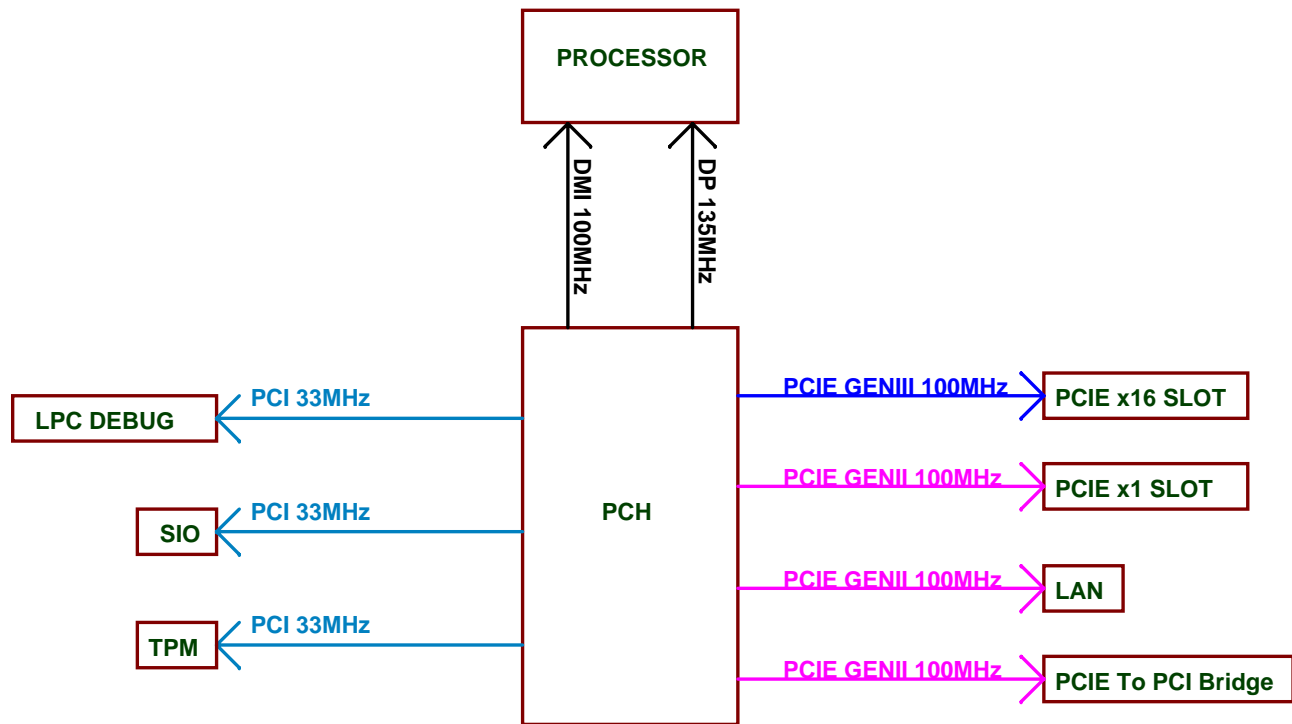
PCI Express x16 Slot * 1

PCI Express x1 Slot * 2

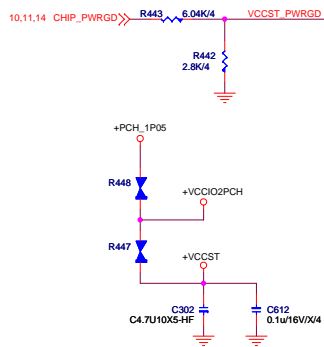
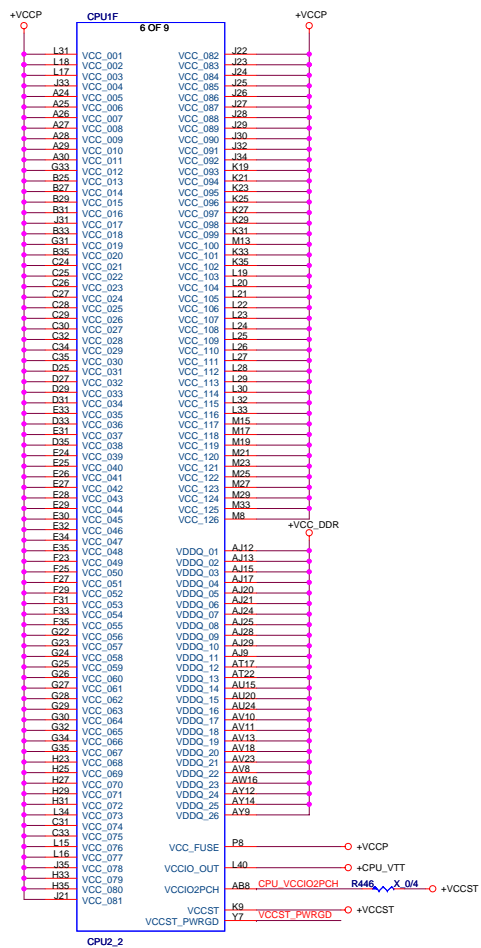
PCI Slot * 1



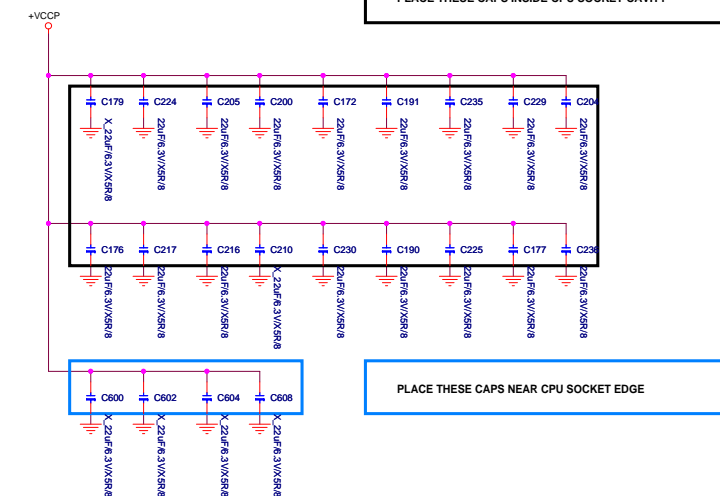




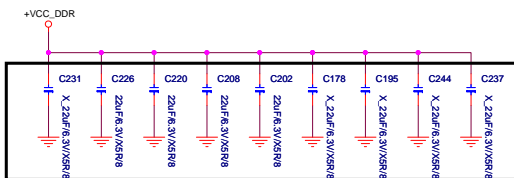


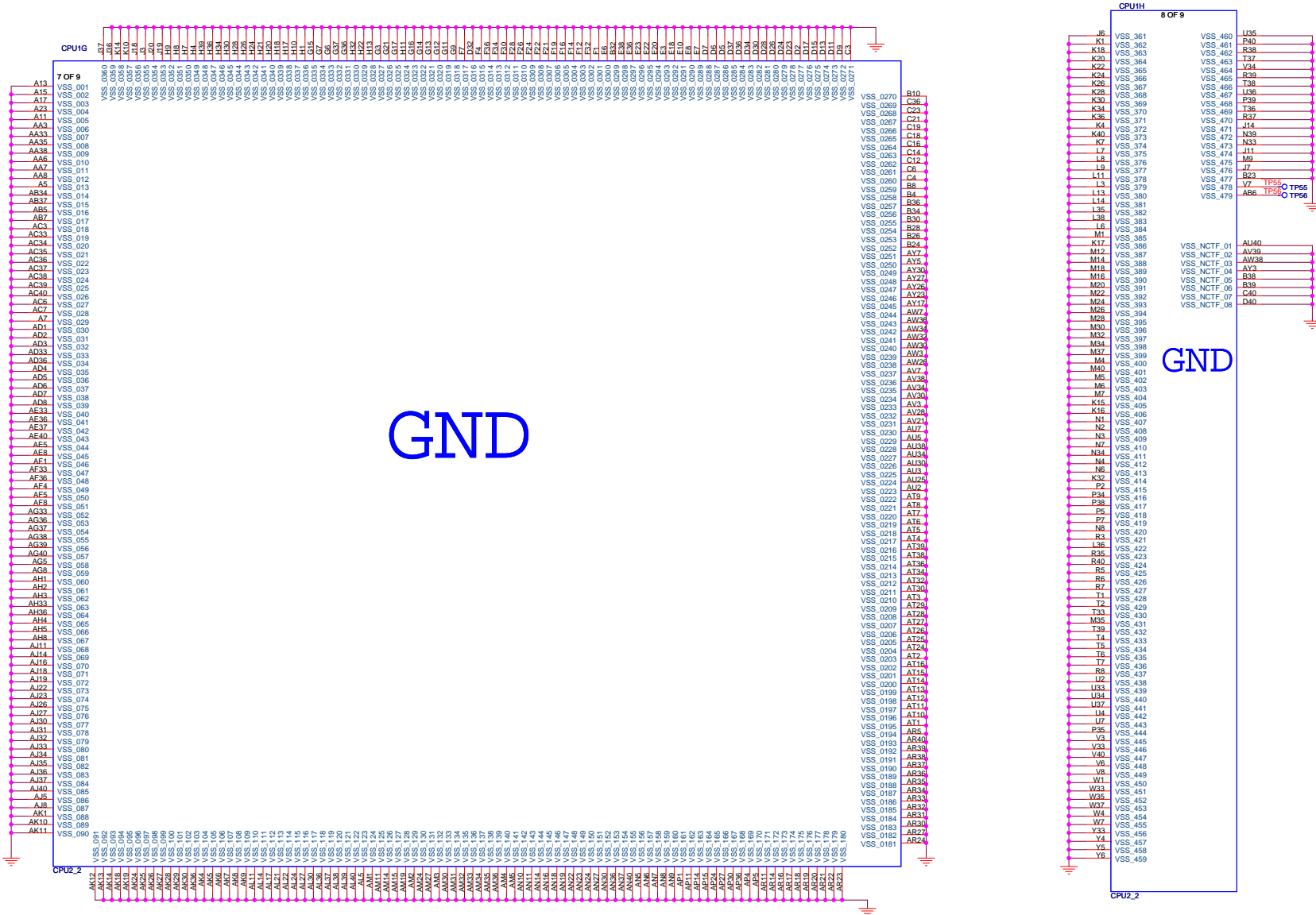


VCCP-Decoupling



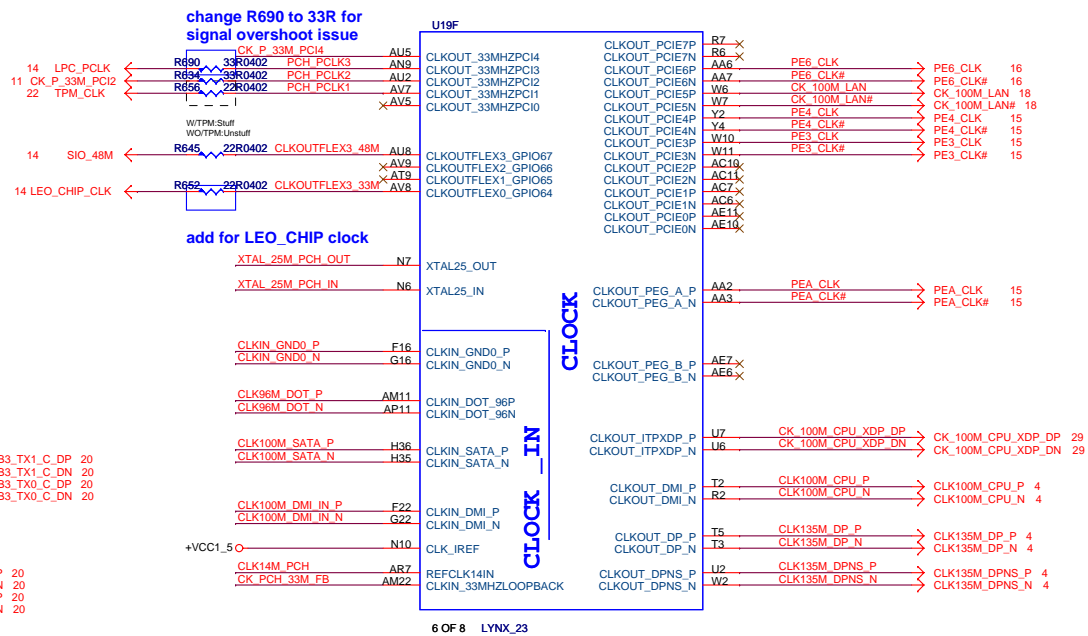
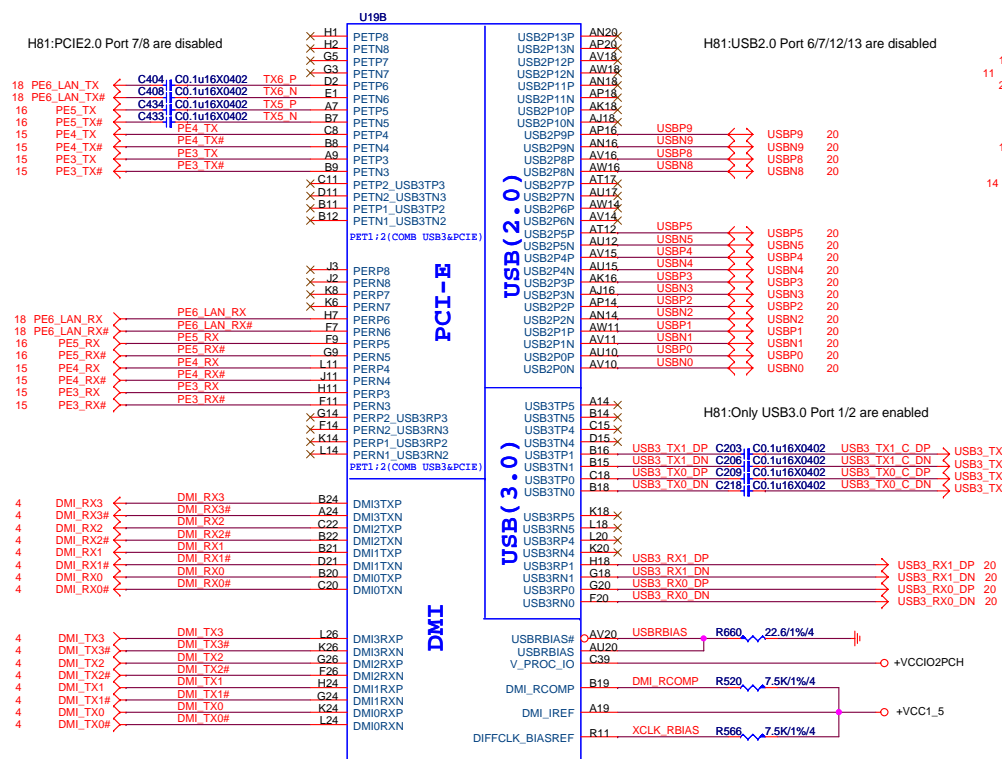
VCC_DDR-Decoupling

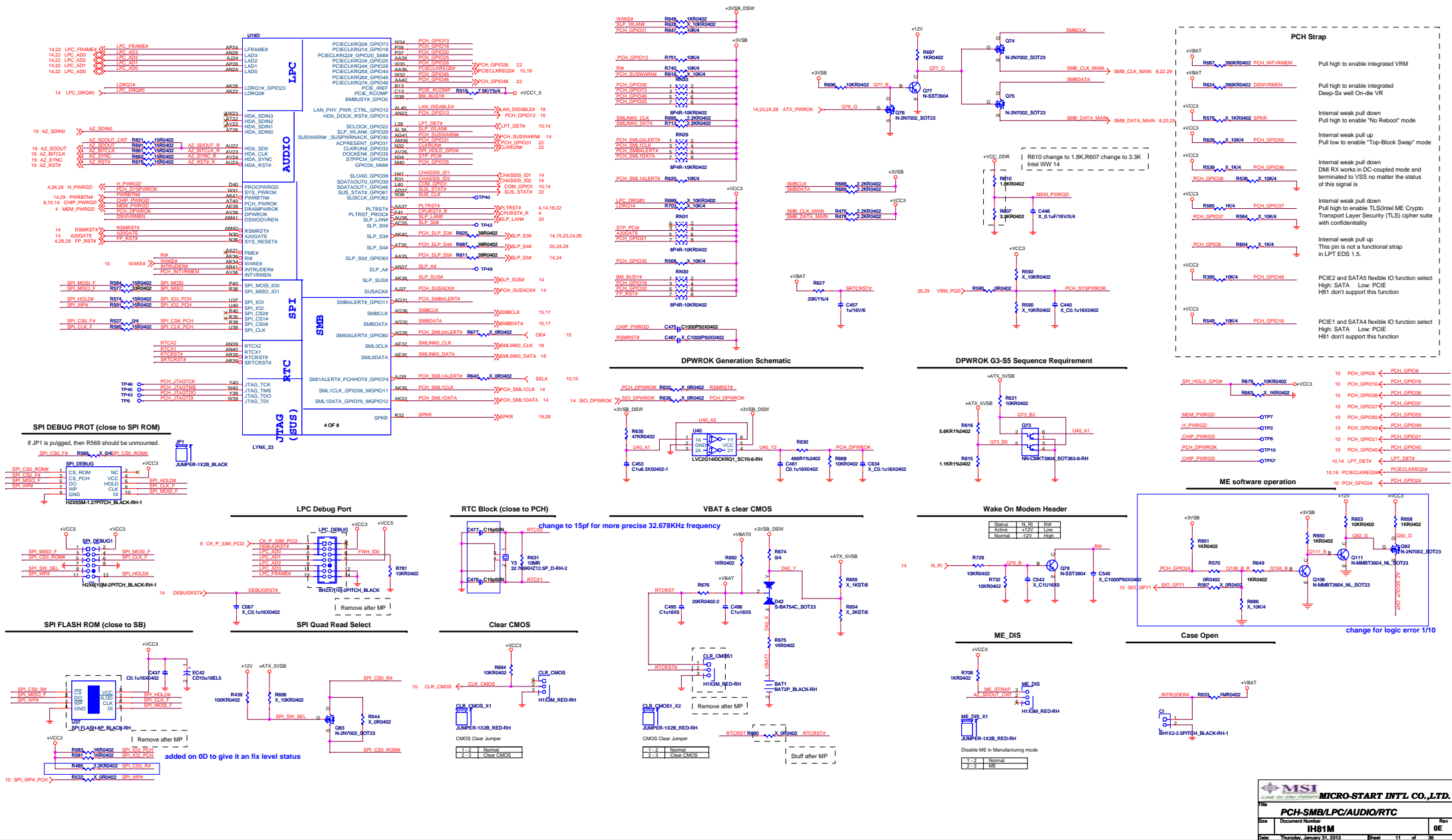




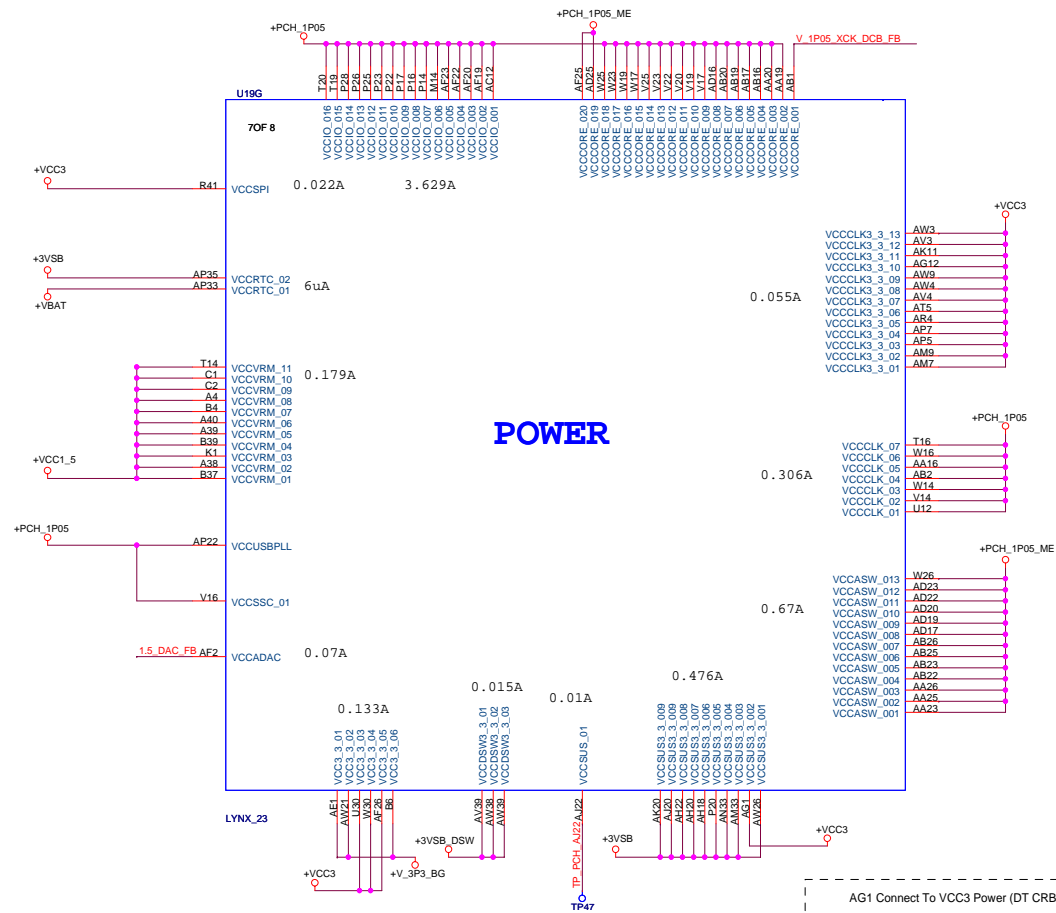
Palce Caps Between CHA And CHB



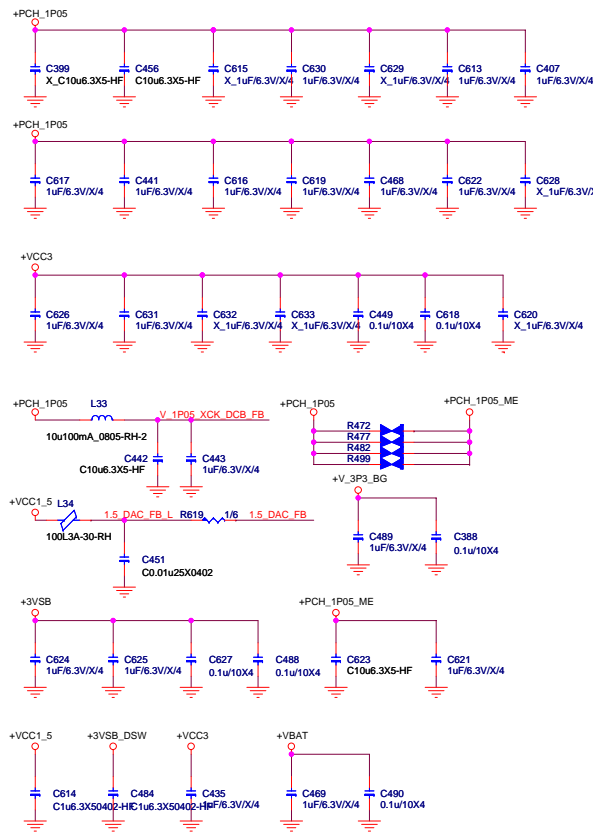




AF25 | AD25 Connect To ASW Power (DT CRB0.7)



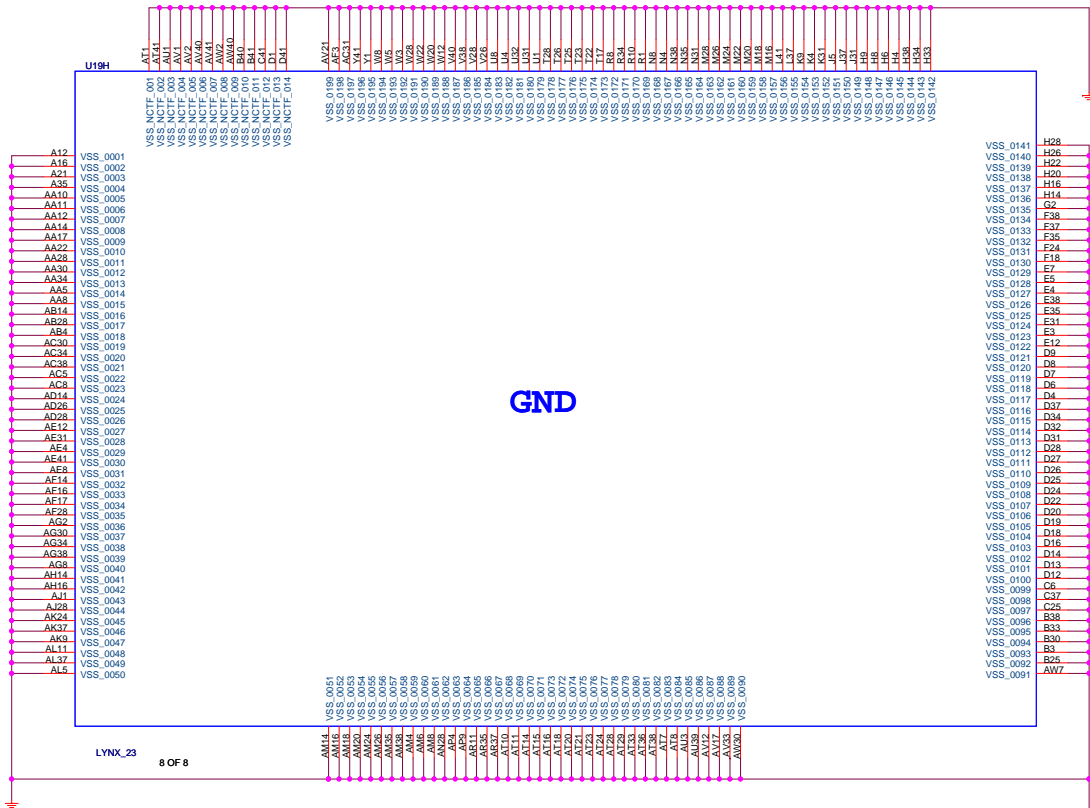
AG1 Connect To VCC3 Power (DT CRB0.7)

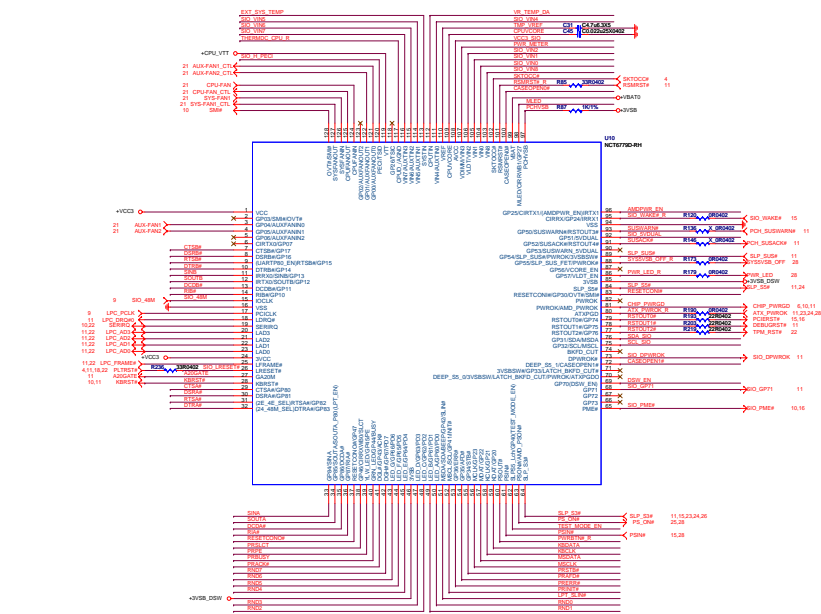


Place C399 | C456 | C615 | C630 | C629 near P14, P16, P17, P26, P28 C613 near M14 C407 near U12 C617 near W14 C441 near AB2 C616 near V16 C619 | C468 near AA16, W16 C622 | C628 near AP22, AF19

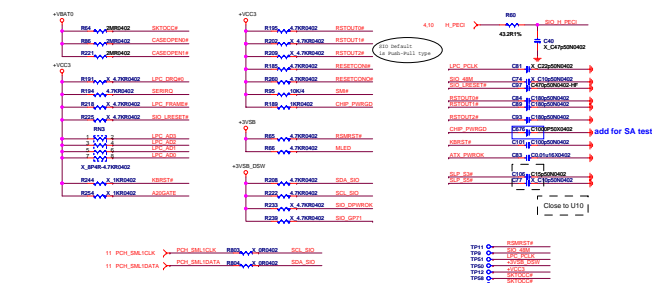
Place C626 | C631 | C632 | C633 near AV4, AR4, AT5, AP5 C449 near AG1 C618 near W30 C620 near AF26 Place C627 near AN33 C624 near AK20 C488 near AW26 C625 near AP35

Place C614 near T14 Place C484 near AW39 Place C435 near R41 Place C623 | C621 near AD17, AD19 Place C489 near AW21 C388 near B6





Required Pull Up And Pull Low



3V Analog Power



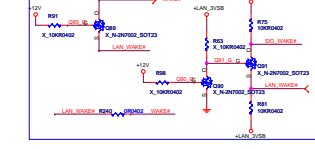
Pwrbtn# Schematic



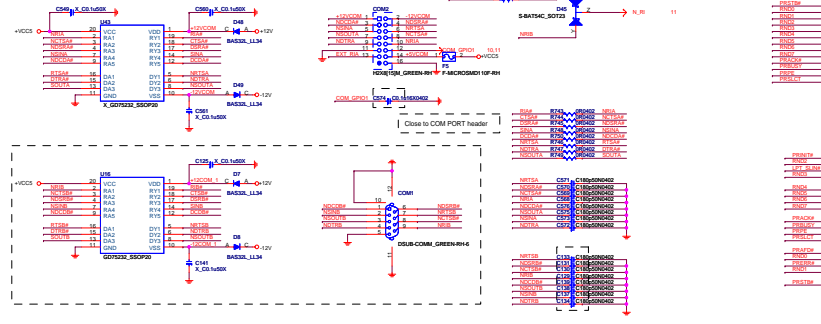
SIO Power Decoupling



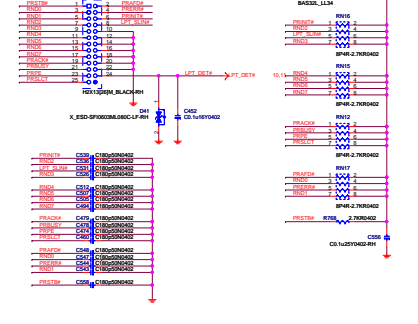
LAN Wake UP



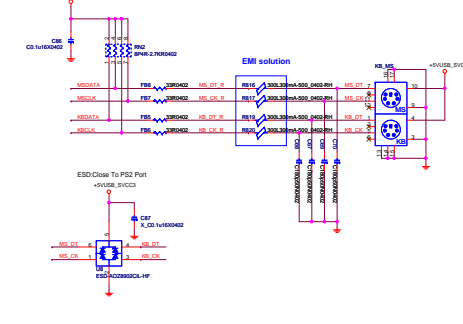
COM Port and Pin Header



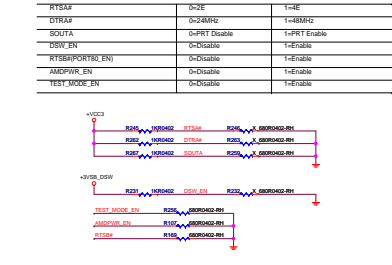
LPT Pin Header



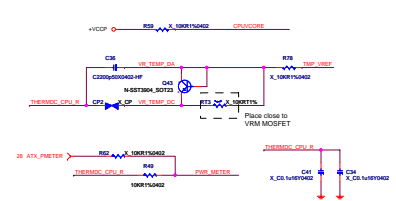
PS2 Keyboard/Mouse Pin Header



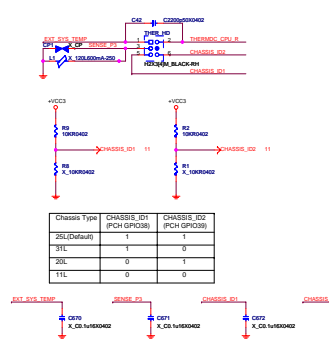
SIO Pin Strap



Voltage And Temp Sensing



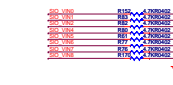
System Sensor Header



SIO DSW Sequence

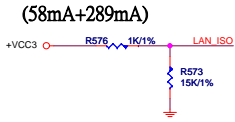
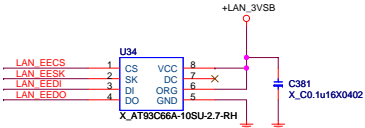
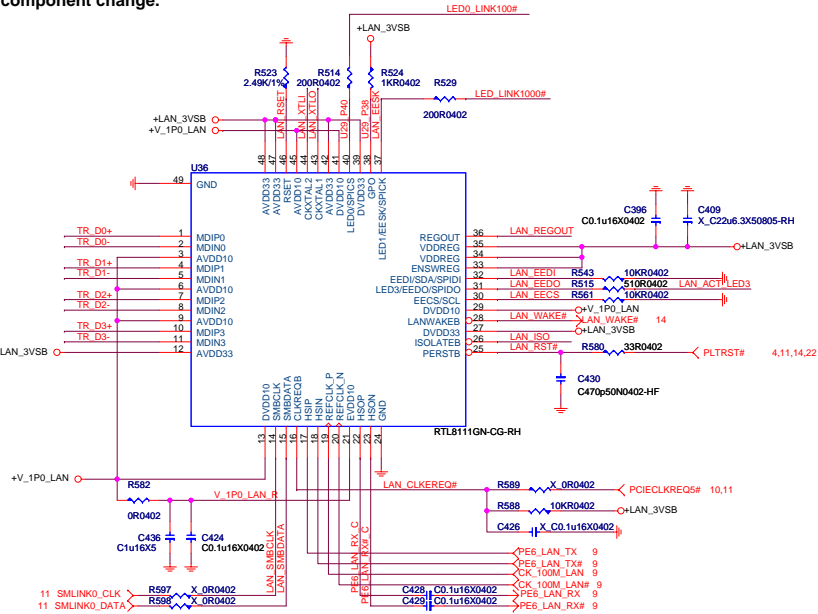


VIN Detect



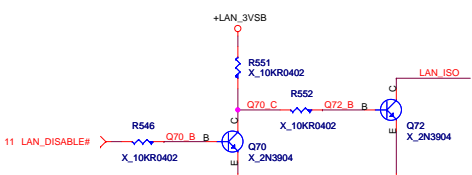
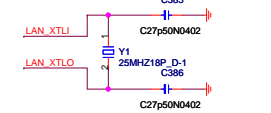
Gigabit LAN RTL8111E-VC Co-lay RTL8111GN

RTL8111E-VC is pin to pin compatible with RTL8111GN.
The two chips can change each other without any component change.



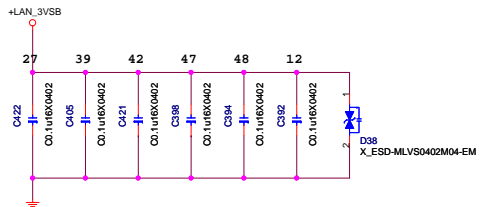
WOL	status	Yellow	Gm/Org
don't care	No Link	off	off
off	S3/S4/S5	off	off
on	S3/S4/S5	off	off
on	10M.inactive		off
on	10M.active		
on	100M.inactive		
on	100M.active		
on	1G.inactive		
on	1G.active		

always on
always on
always on
blinking

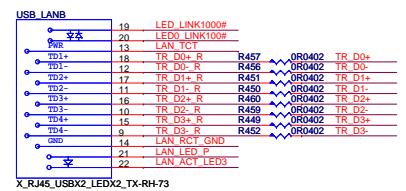


EMI solution: can be unmounted if LAN connector has surge protect

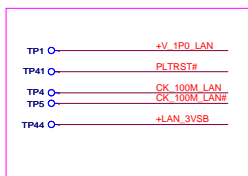
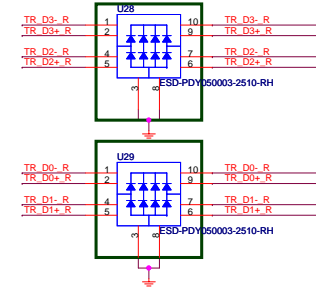
Place Near Pin



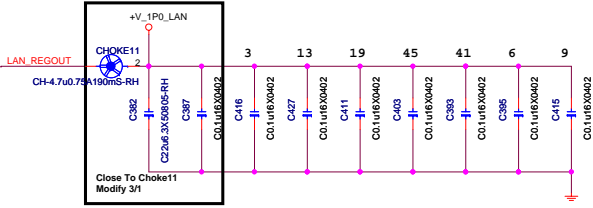
LAN Connector



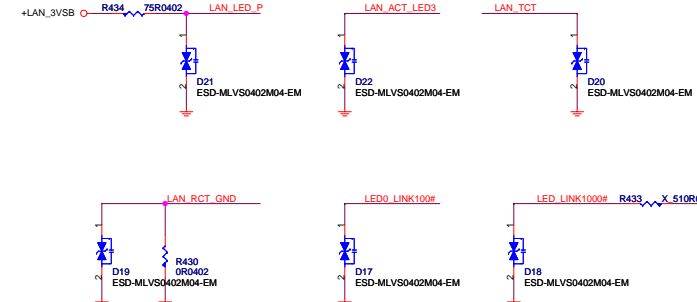
ESD



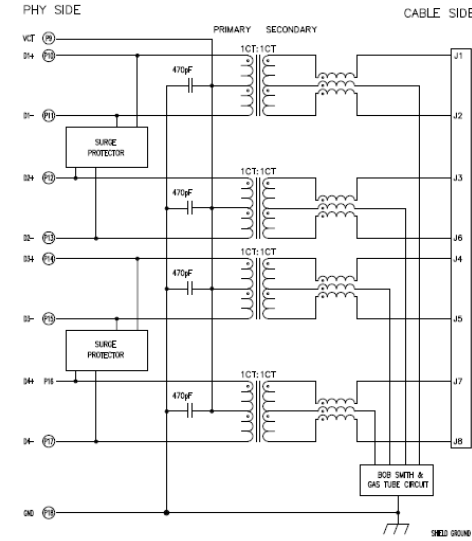
Place Near Pin



ESD

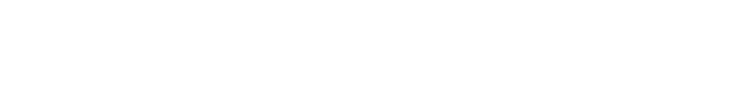
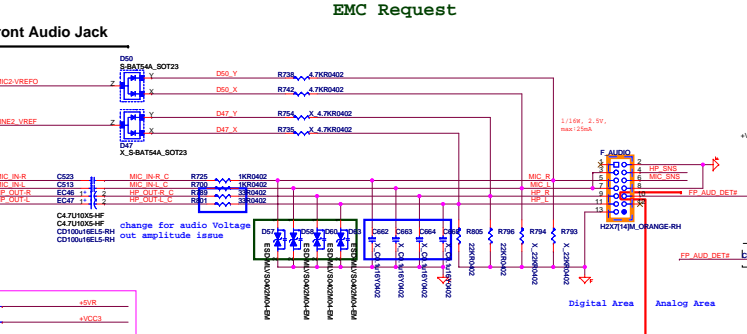
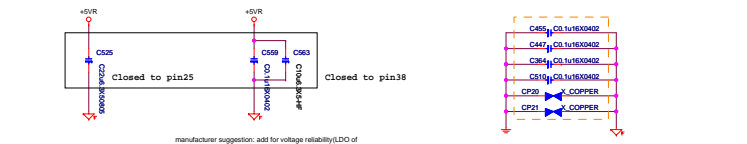
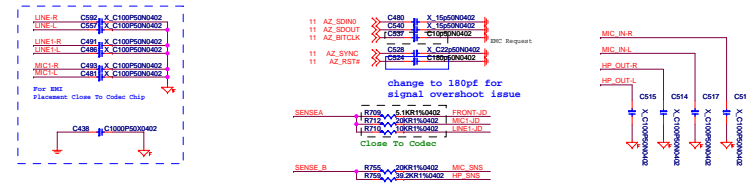
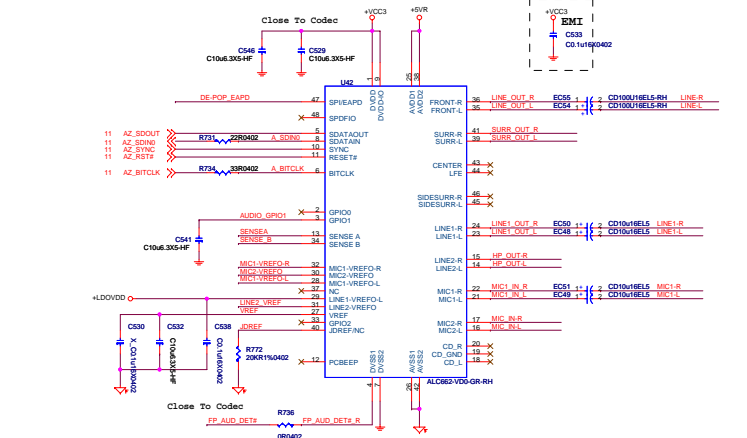


SCHEMATIC

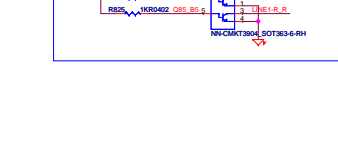
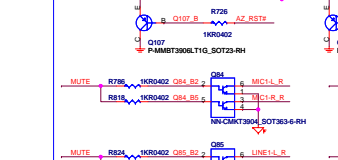
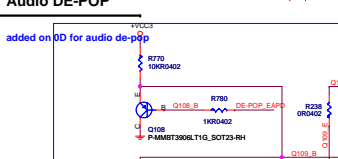
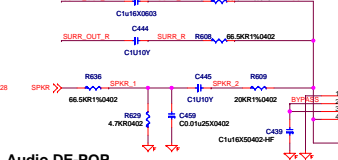
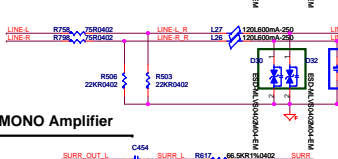
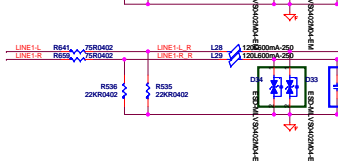
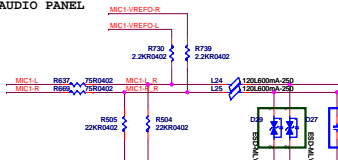
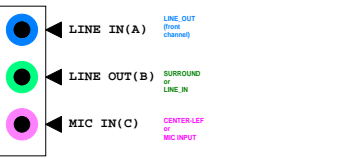
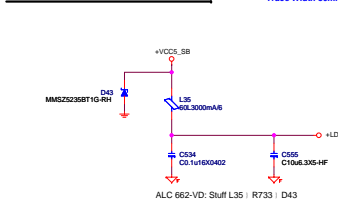


Azalia Codec - ALC662-VD

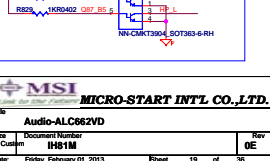
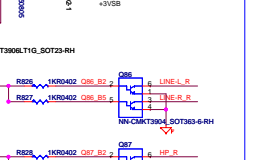
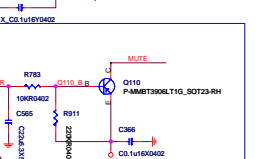
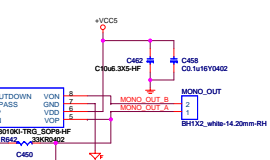
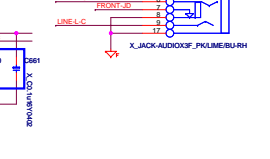
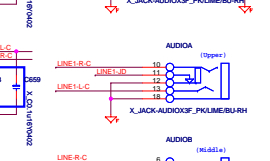
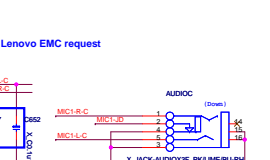
removed ALC662VC co-layer schematic on OD



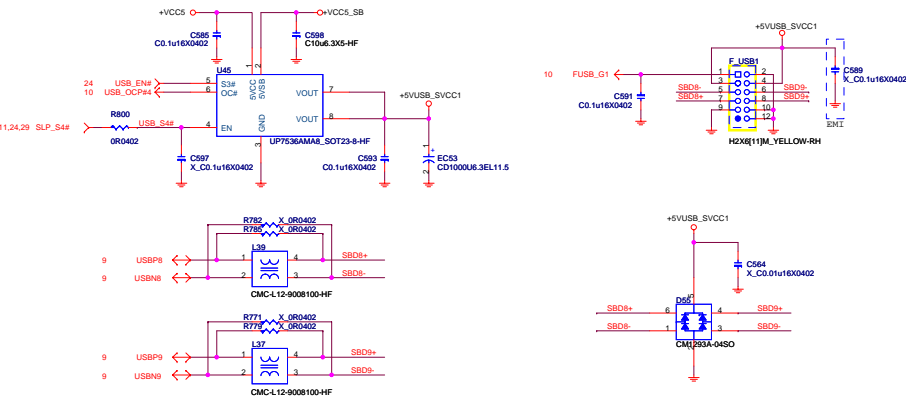
AUDIO CODE REGULATORS



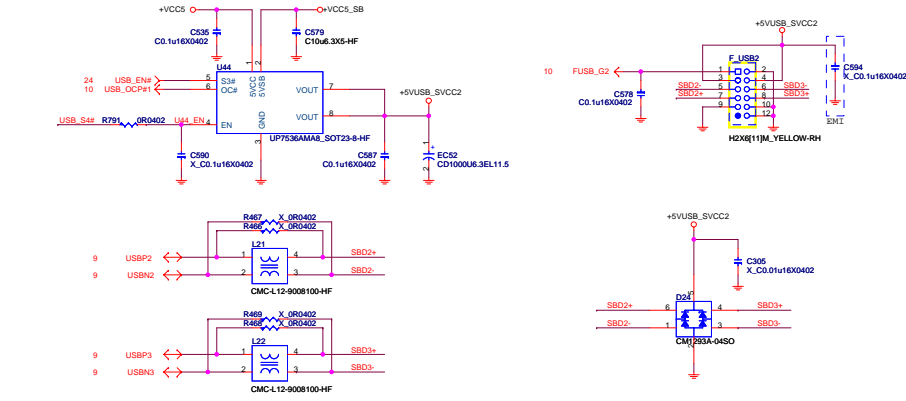
Trace Width 30mils.



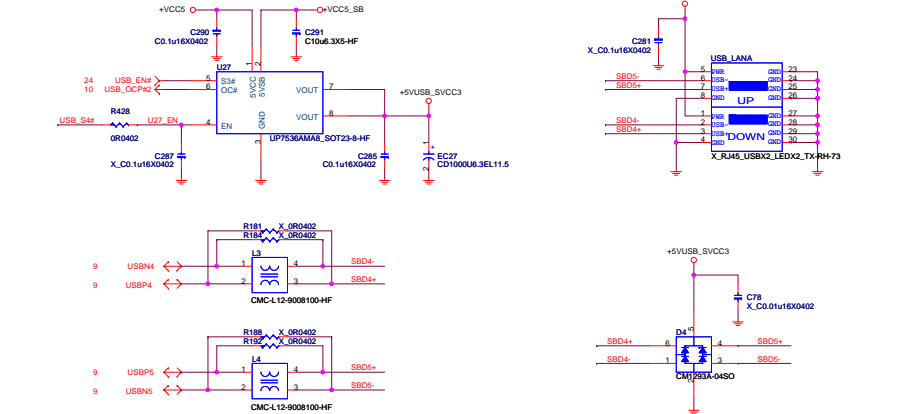
Front Panel USB Connector For USB Port 6 / 7



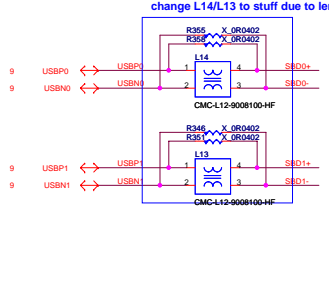
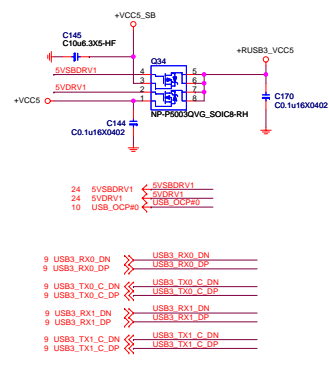
Front Panel USB Connector For USB Port 2 / 3



Rear USB Connector For USB Port 2 / 3



Rear USB Connector For USB Port 0 / 1



SATA1

10 SATA_RX0 ← C466 C0.01u16X0402 S_RX0
 10 SATA_RX0 ← C465 C0.01u16X0402 S_RX0
 10 SATA_TX0 ← C464 C0.01u16X0402 S_TX0
 10 SATA_TX0 ← C463 C0.01u16X0402 S_TX0

SATA7PM_RED-ST-RH-1

SATA2

10 SATA_RX1 ← C473 C0.01u16X0402 S_RX1
 10 SATA_RX1 ← C472 C0.01u16X0402 S_RX1
 10 SATA_TX1 ← C471 C0.01u16X0402 S_TX1
 10 SATA_TX1 ← C470 C0.01u16X0402 S_TX1

SATA7PM_RED-ST-RH-1

SATA3

10 SATA_RX4 ← C500 C0.01u16X0402 S_RX4
 10 SATA_RX4 ← C499 C0.01u16X0402 S_RX4
 10 SATA_TX4 ← C498 C0.01u16X0402 S_TX4
 10 SATA_TX4 ← C497 C0.01u16X0402 S_TX4

SATA7PM_ORANGE-P-RH

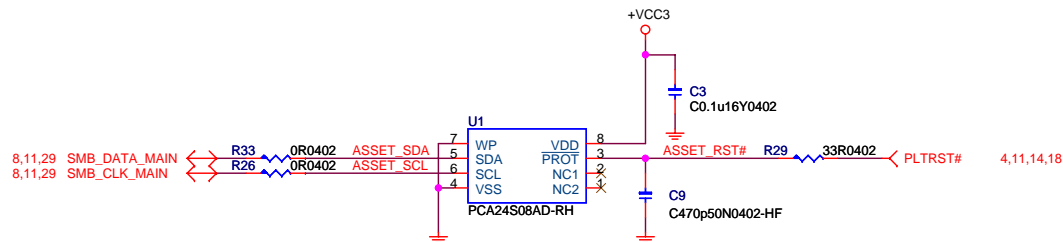
SATA4

10 SATA_RX5 ← C504 C0.01u16X0402 S_RX5
 10 SATA_RX5 ← C503 C0.01u16X0402 S_RX5
 10 SATA_TX5 ← C502 C0.01u16X0402 S_TX5
 10 SATA_TX5 ← C501 C0.01u16X0402 S_TX5

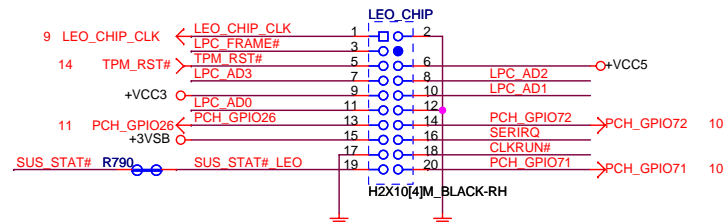
SATA7PM_ORANGE-P-RH

[illegible][illegible][illegible]

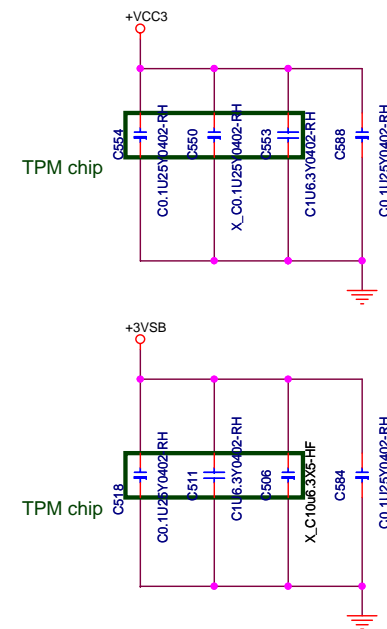
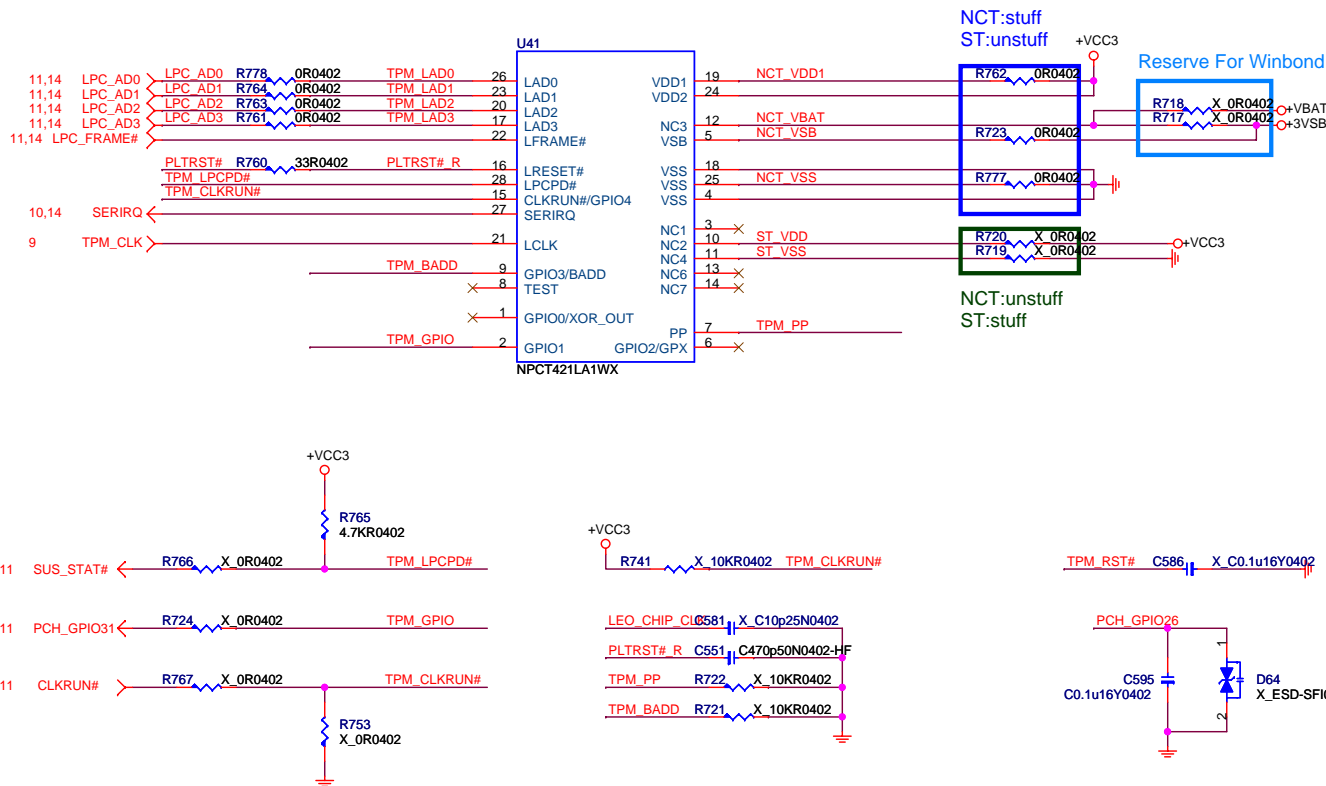
Asset ID



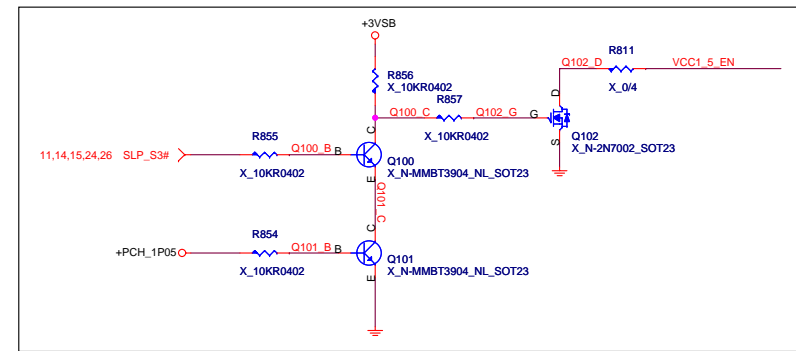
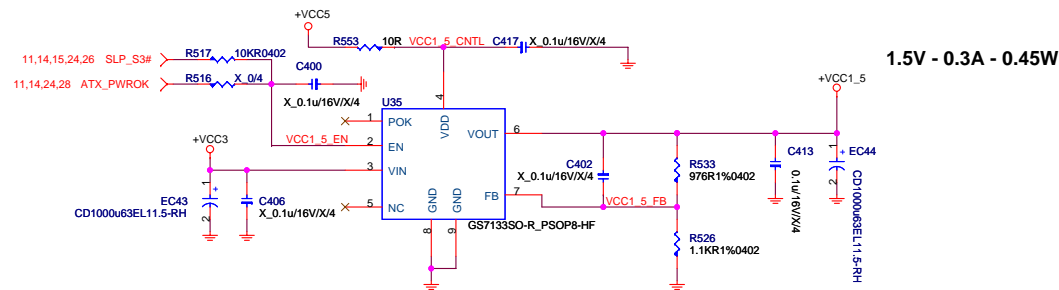
TCM Header



TPM



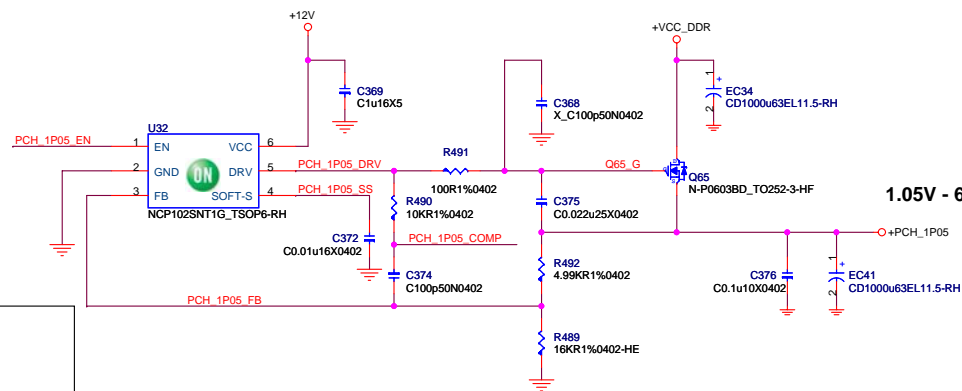
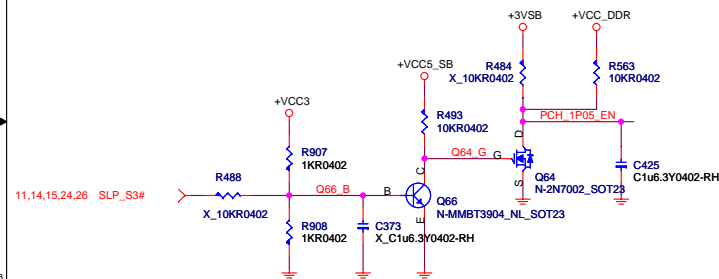
1.5V Power




sequence requirement on VCC1_5 and PCH_1P05

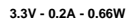
PCH Core Power Control

PCH Core Power

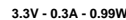


VCC3_3 pins on the Core well (AE1, B6, AW21) have a sequencing requirement with respect to the PCH Core 1.05V rail (VCC)

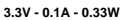
 MICRO-START INT'L CO.,LTD.		
Title		
PCH & ME Core Power		
Size	Document Number	Rev
	IH81M	0E
Date:	Friday, January 11, 2013	Sheet 23 of 36

$$V_{out} = 0.8[(R_{254} + R_{246}) / R_{254}]$$


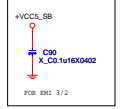
AVL: I31-7133S02-N03/I31-3730S02-N62



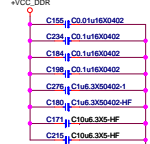
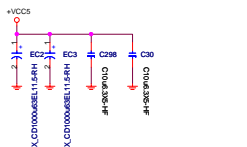
change LAN power source to 3VSB as it don't need power in deep S5

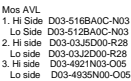


5V - 7.5A - 37.5W



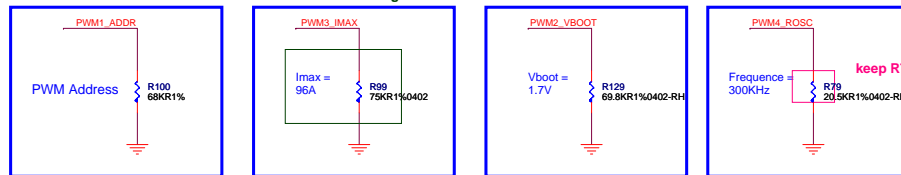
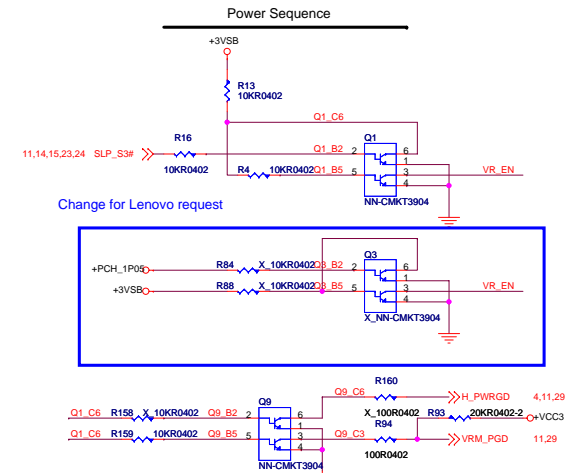
0.75V - 1.1A - 0.825W





SKIP

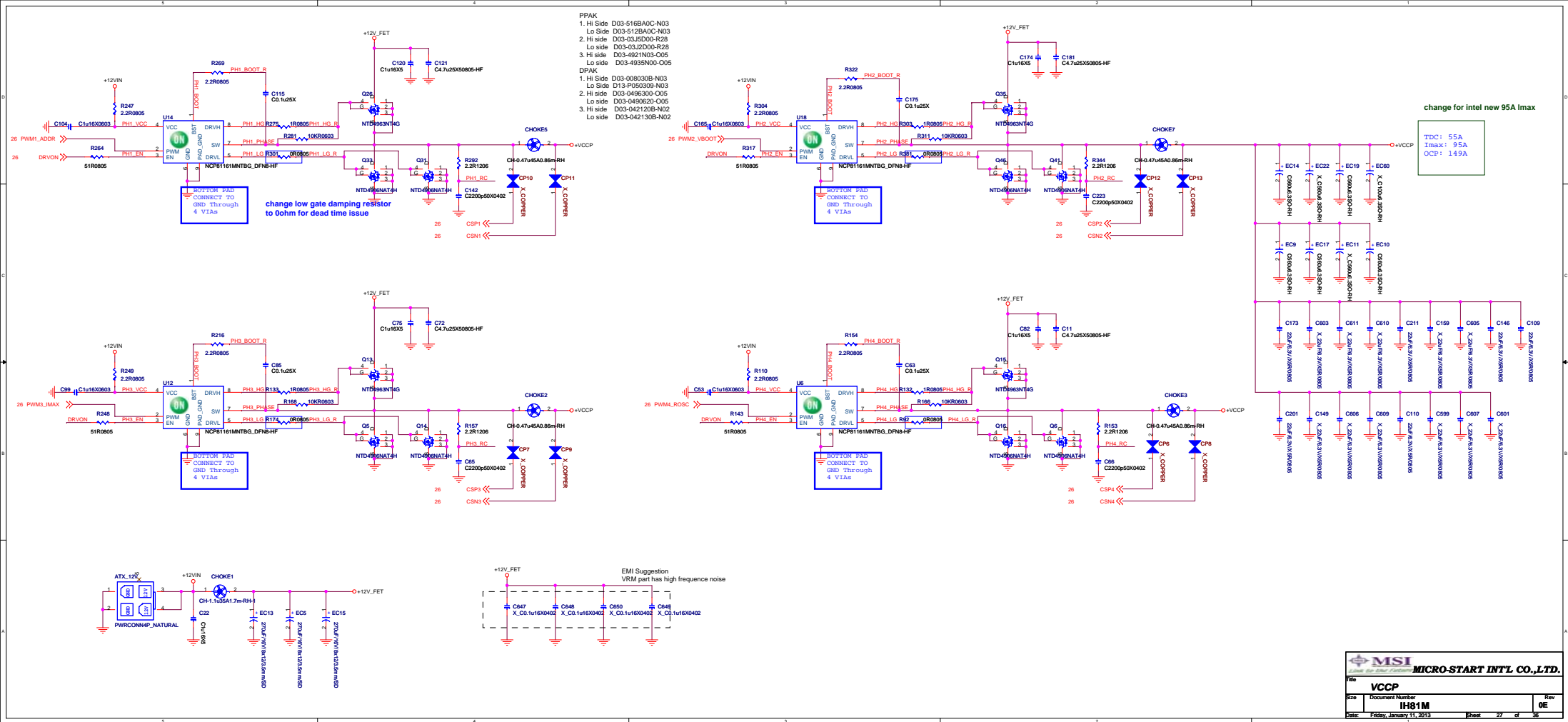




Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.
10K	250Kh	30.9K	340Khz	61.9K	430Khz	105K	520 Khz	165K	610Khz
12K	260Kh	34K	350Khz	64.9K	440Khz	110K	530Khz	174K	620Khz
14K	270Kh	36.5K	360Khz	69.8K	450Khz	115K	540Khz	182K	630Khz
16.2K	280Kh	40.2K	370Khz	73.2K	460Khz	121K	550Khz	191K	640Khz
18.2K	290Kh	43.2K	380Khz	78.7K	470Khz	130K	560Khz	200K	650Khz
20.5K	300Kh	46.4K	390Khz	82.5K	480Khz	137K	570Khz		
23.2K	310Kh	49.9K	400Khz	88.7K	490Khz	143K	580Khz		
25.5K	320Kh	53.6K	410Khz	93.1K	500Khz	150 K	590Khz		
28K	330Kh	57.6K	420Khz	100K	510Khz	158 K	600Khz		

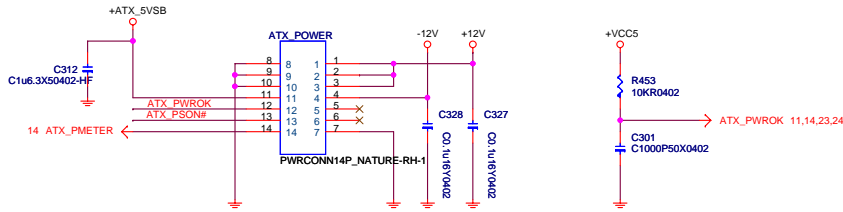
PWM ADDRESS	
RESISTOR VALUE	SVID ADDRESS FOR VCORE RAIL
10K	0000
25K	0010
45K	0100
70K	0110
95K	1000
125K	1010
165K	1100

BOOT VOLTAGE & Phase no.		
RESISTOR VALUE	BOOT VOLTAGE	Phase no in PS1
30.1K	1.0V	1
49.9K	1.65V	1
69.8K	1.7V	1
90K	1.75V	1
130K	1.0V	2
150K	1.65V	2
169K	1.7V	2
open	1.75V	2



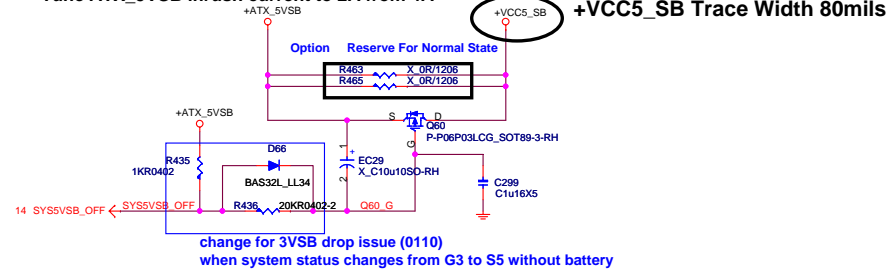
ATX Power Connector / Front Panel / LED/DSW

14 Pin ATX Power Connector

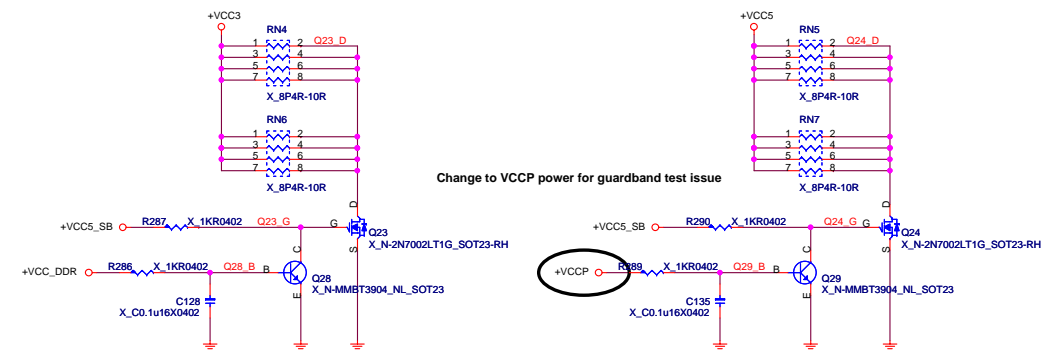


5VSB Power Switch

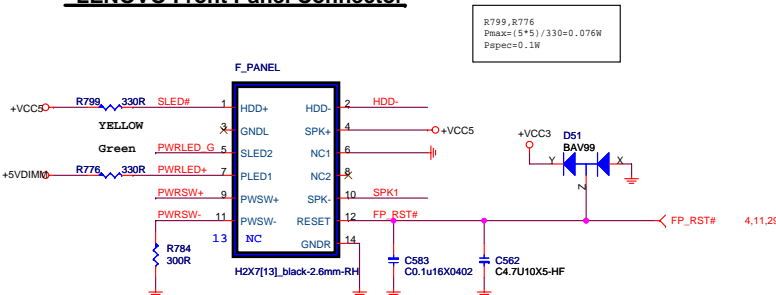
Tune ATX_5VSB inrush current to 2A from 4A



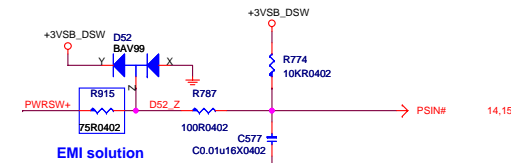
VCC3 } VCC5 Discharge Schematic



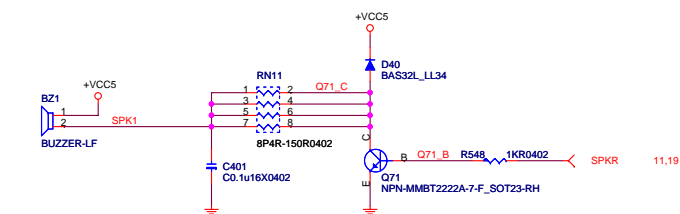
LENOVO Front Panel Connector



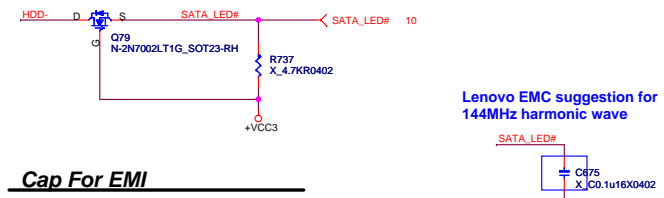
Power Button



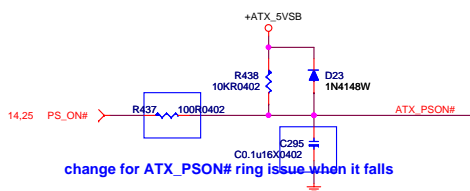
Buzzer Circuit



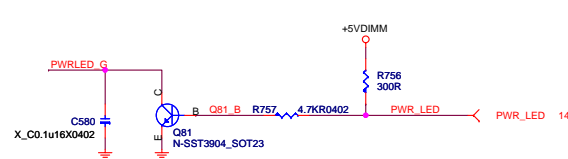
HDD LED



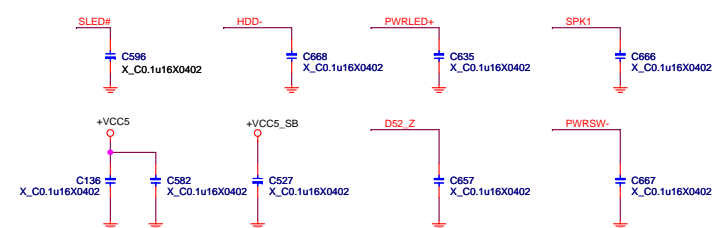
ATX Power On



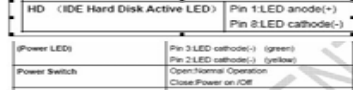
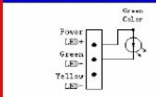
Power LED



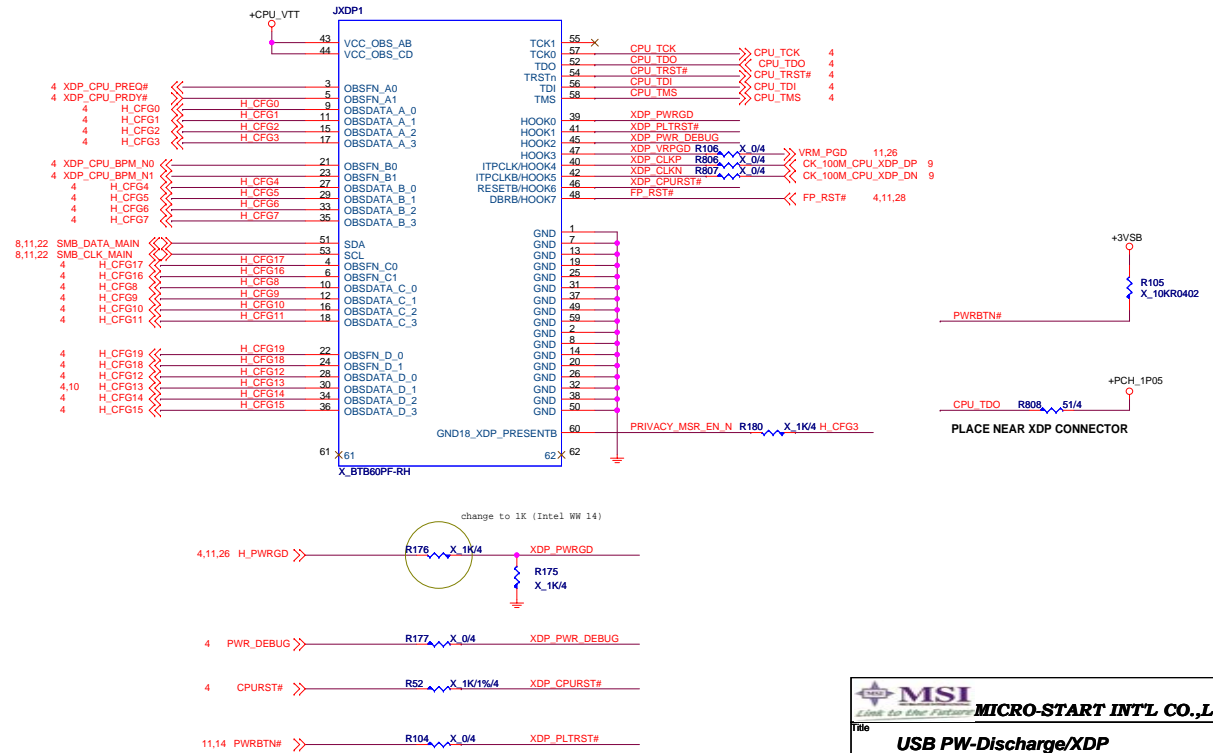
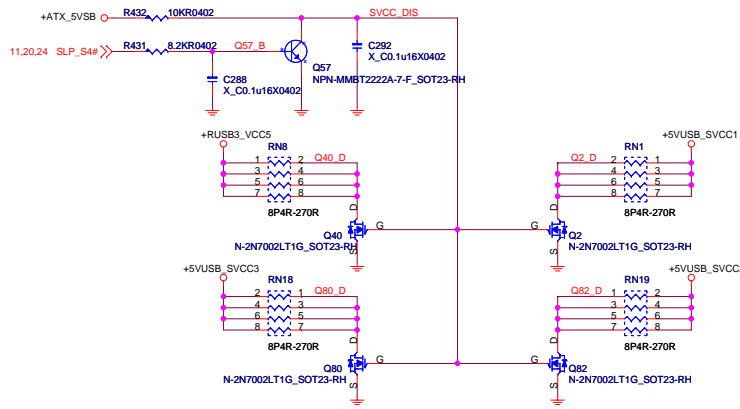
Cap For EMI



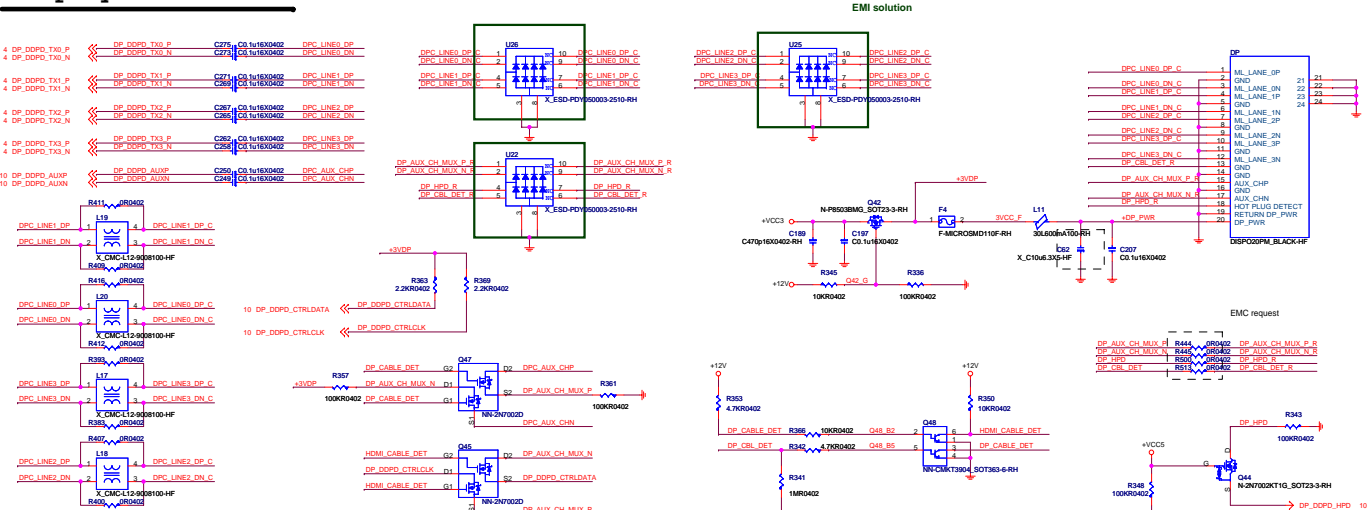
2-pin single color Power LED



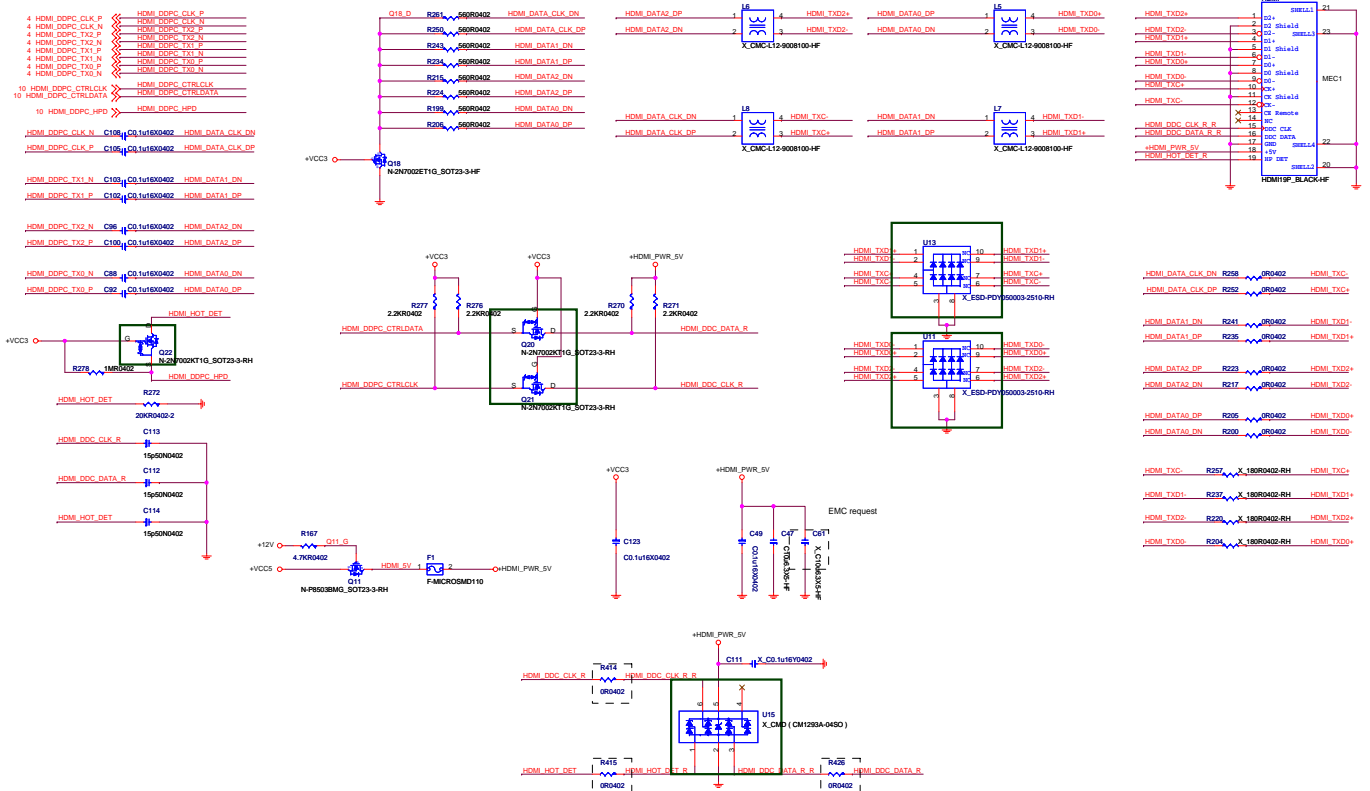
Reserve debug port 5020

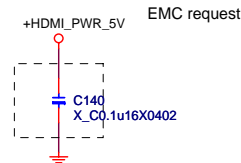
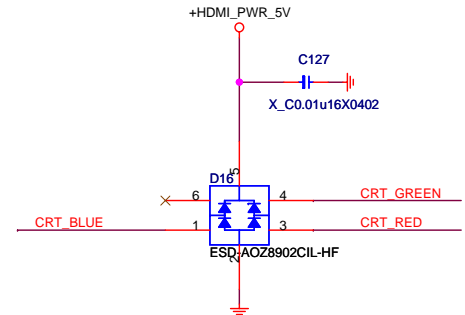
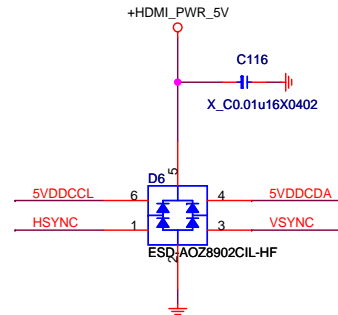
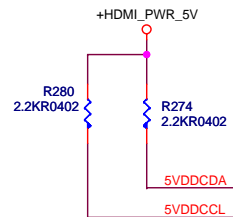
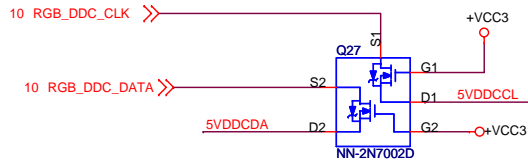
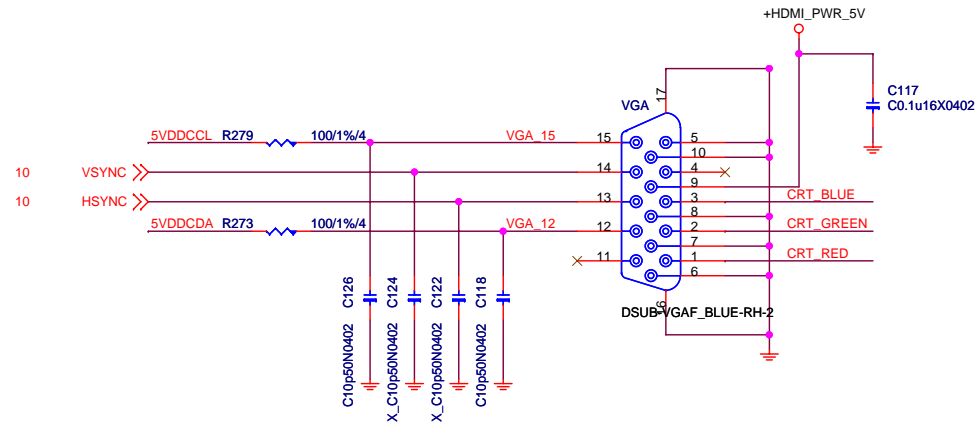
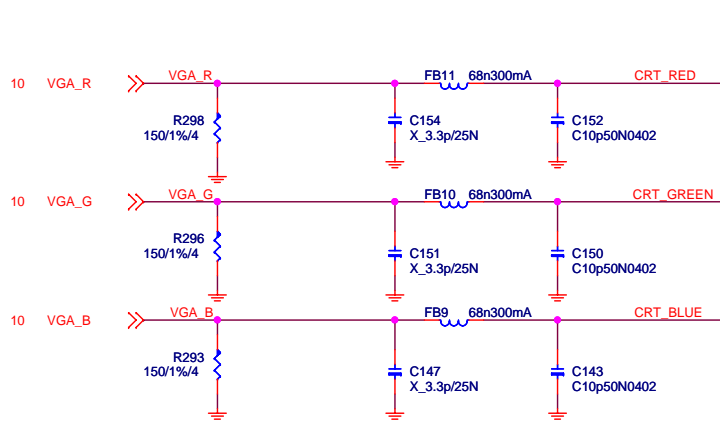


Display Port

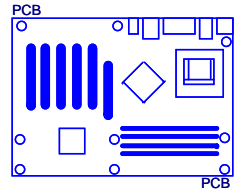


HDMI Port

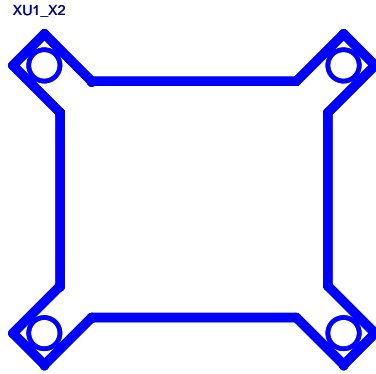




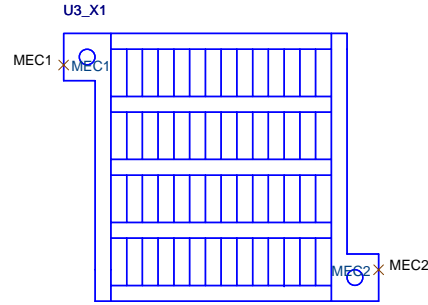
Manual Parts



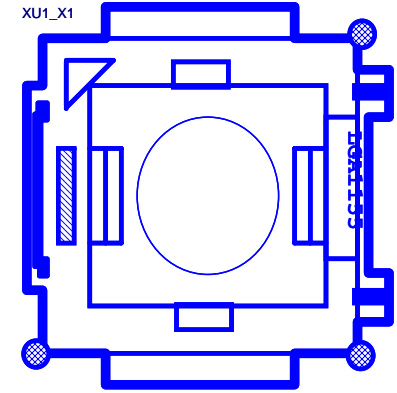
P30-0782510-E48/P30-0782510-E55



X_CPU Backplate

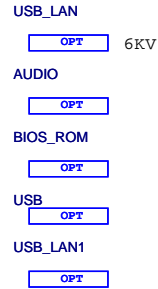
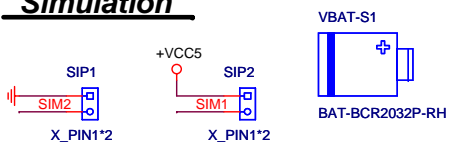


PCH Heatsink

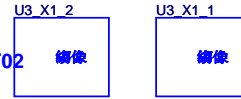


CPU SOCKET

Simulation

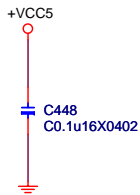


change LAN connector to N58-22F1691-F02 to use sidactor for surge protection

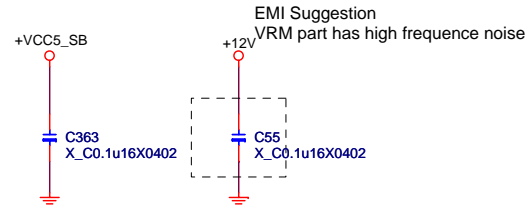
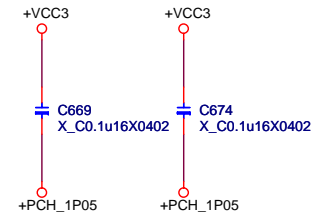


add without surge connector for Malmo and Toulouse without LAN surge: N58-22F1371-F02/N58-22F1321-I60/N58-22F1331-U30/N58-22F1351-S42

For EMI



For Moat CAP

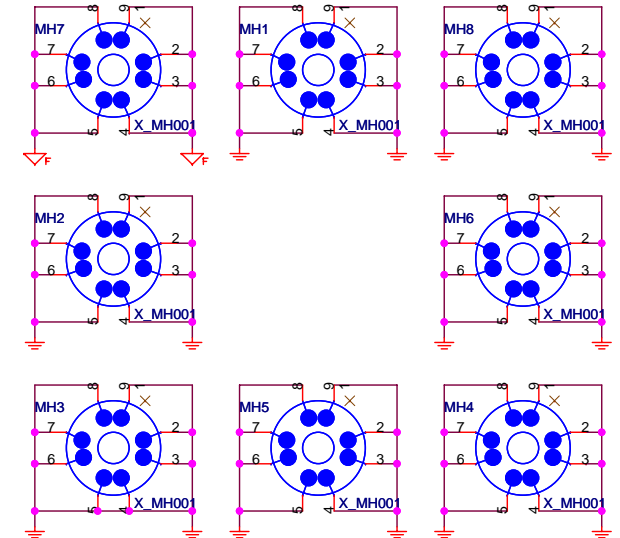


Optics Orientation Holes

Optical Fiducial Marks-120



Mounting Holes



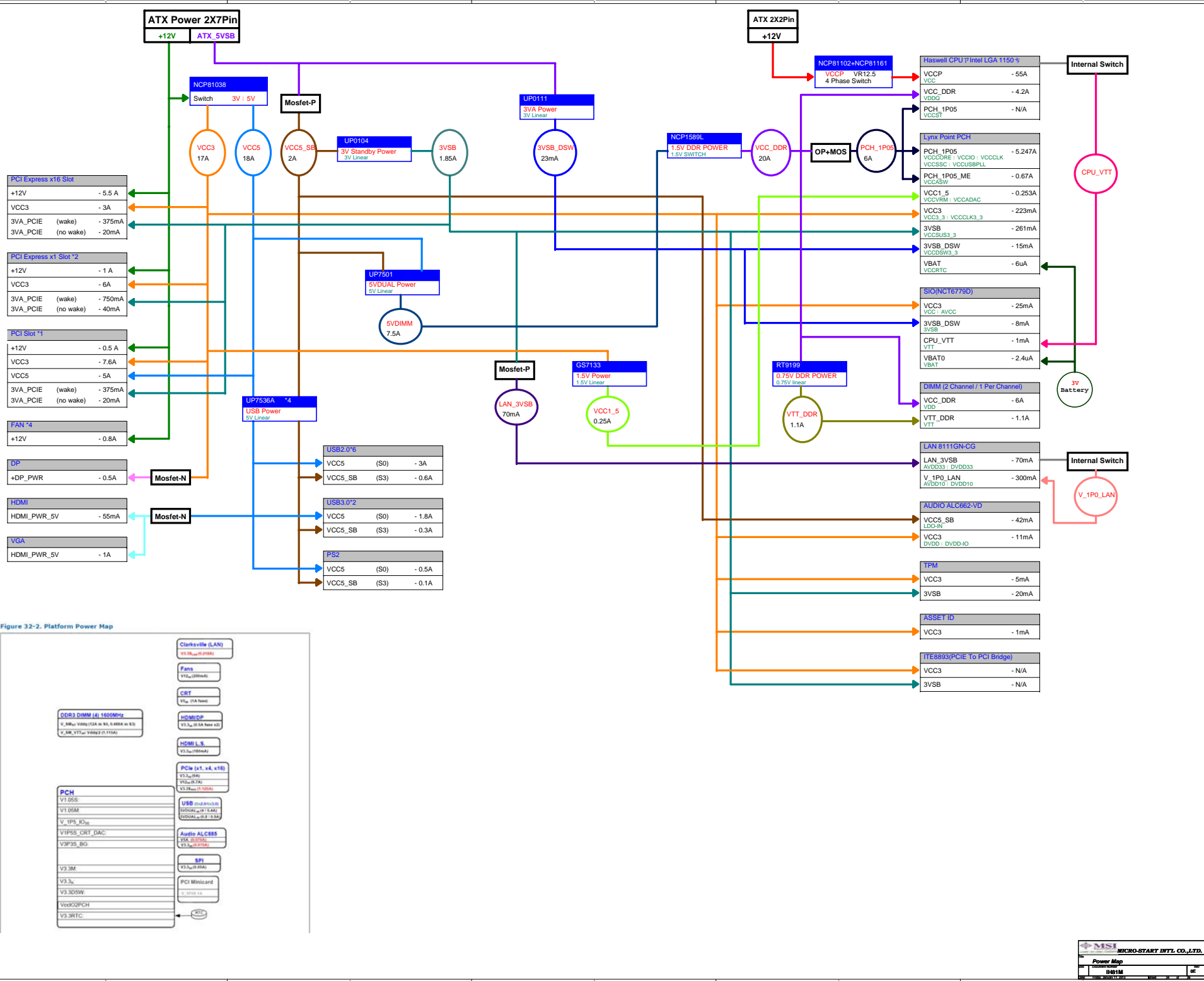


Figure 32-2. Platform Power Map

PCH								
GPIO	Alt Function	I/O/NC	Power	Tol	Default	Signal Name	Input/Output	Pull-Hi/Pull-Low
GPIO[0]	BMBUSY#	I/O	Main	3.3V	GPI	BM_BUSY#	Input	Pull-Hi
GPIO[1]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO1	Input	Pull-Hi
GPIO[2]	PIRQE#	I/O	Main	5V	GPI	SPL_WP#_PCH	Output	Pull-Hi
GPIO[3]	PIRQF#	I/O	Main	5V	GPI	PCH_GPIO3	Input	Pull-Hi
GPIO[4]	PIRQG#	I/O	Main	5V	GPI	PCH_GPIO4	Input	Pull-Hi
GPIO[5]	PIRQH#	I/O	Main	5V	GPI	PCH_GPIO5	Input	Pull-Hi
GPIO[6]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO6	Input	Pull-Hi
GPIO[7]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO7	Input	Pull-Hi
GPIO[8]	Unmuxed	I/O	Resume	3.3V	GPO	PCH_GPIO8	Output	Pull-Hi
GPIO[9]	OC5#	I/O	Resume	3.3V	Native	USB_OC#5	Input	Pull-Hi
GPIO[10]	OC6#	I/O	Resume	3.3V	Native	USB_OC#6	Input	Pull-Hi
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	PCH_SMBALERT#	Output	Pull-Hi
GPIO[12]	LAN_PHY_PWR_CTRL	I/O	Resume	3.3V	Native	LAN_DISABLE#	Output	NC
GPIO[13]	Unmuxed	I/O	Resume	3.3V	GPI	PCH_GPIO13	Output	Pull-Hi
GPIO[14]	OC7#	I/O	Resume	3.3V	Native	SIO_PME#	Input	Pull-Hi
GPIO[15]	Unmuxed	I/O	Resume	3.3V	GPO	PCH_GPIO15	Output	Pull-Hi
GPIO[16]	SATA4GP	I/O	Main	3.3V	GPI	PCH_GPIO16	Input	Pull-Hi
GPIO[17]	Unmuxed	I/O	Main	3.3V	GPI	CLR_CMOS	Input	Pull-Hi
GPIO[18]	PCIECLKRQ1#	I/O	Main	3.3V	Native	PCH_GPIO18	Input	Pull-Hi
GPIO[19]	SATA1GP	I/O	Main	3.3V	GPI	PCH_GPIO19	Input	Pull-Hi
GPIO[20]	PCIECLKRQ2#	I/O	Main	3.3V	Native	PCIECLKREQ2#	Input	Pull-Hi
GPIO[21]	SATA0GP	I/O	Main	3.3V	GPI	PCH_GPIO21	Input	Pull-Hi
GPIO[22]	SCLOCK	I/O	Main	3.3V	GPI	LPT_DET#	Input	Pull-Hi
GPIO[23]	LDRQ1#	I/O	Main	3.3V	Native	LDRQ1#	Input	NC
GPIO[24]	Unmuxed	I/O	Resume	3.3V	GPO	PCH_GPIO24	Output	Pull-Low
GPIO[25]	Unmuxed	I/O	Resume	3.3V	Native	PCH_GPIO25	Output	Pull-Hi
GPIO[26]	Unmuxed	I/O	Resume	3.3V	Native	PCH_GPIO26	Input	Pull-Hi
GPIO[27]	Unmuxed	I/O	DSW	3.3V	GPI	PCH_GPIO27	Output	Pull-Hi
GPIO[28]	Unmuxed	I/O	Resume	3.3V	GPO	PCH_GPIO28	Input	Pull-Hi
GPIO[29]	SLP_WLAN#	I/O	Resume	3.3V	Native	SLP_WLAN#	Output	NC
GPIO[30]	SUS_PWRDN_ACK/SUS_WARN#	I/O	Resume	3.3V	GPI	PCH_SUSWARN#	Output	NC
GPIO[31]	Unmuxed	I/O	DSW	3.3V	GPI	PCH_GPIO31	Input	Pull-Hi
GPIO[32]	Unmuxed	I/O	Main	3.3V	GPO	CLKRUN#	Output	NC
GPIO[33]	HDA_DOCK_EN#	I/O	Main	3.3V	GPO	SPL_HOLD_GPO#	Output	Pull-Hi
GPIO[34]	STP_PCI	I/O	Main	3.3V	GPI	STP_PCI#	Input	Pull-Hi
GPIO[35]	Unmuxed	I/O	Main	3.3V	GPO	PCH_GPIO35	Output	NC
GPIO[36]	SATA2GP	I/O	Main	3.3V	GPI	PCH_GPIO36	Input	NC

SIO(NCT6779D)

PIN NAME	USAGE	Input/Output	NOTES
GPIO0	AUX-FAN1_CTL	Output	Fan speed control
GPIO1	NA	NA	NA
GPIO2	NA	NA	NA
GPIO3	NA	NA	NA
GPIO4	AUX-FAN1	Input	Fan speed sense
GPIO5	NA	NA	NA
GPIO6	NA	NA	NA
GPIO7	NA	NA	NA
GPIO10	RIB#	Input	Com port signal
GPIO11	DCDB#	Input	Com port signal
GPIO12	SOUTB	Output	Com port signal
GPIO13	SINB	Input	Com port signal
GPIO14	DTRB#	Output	Com port signal
GPIO15	RTSB#	Output	Com port signal
GPIO16	DSRB#	Input	Com port signal
GPIO17	CTSB#	Input	Com port signal
GPIO20	KBDATA	Input	Keyboard data in
GPIO21	KBCLK	Output	keyboard clock out
GPIO22	MSDATA	Input	Mouse data in
GPIO23	MSCLK	Output	Mouse clock out
GPIO24	SIO_WAKE#_R	Input	Wake up signal from LAN
GPIO25	AMDPWR_EN	Input	Pin strap which disabled AMD power sequence
GPIO26	NA	NA	NA
GPIO27	MLED	Output	Pull high
GPIO30	RESETCON#	Input	Pull high
GPIO31	SDA_SIO	Output	Pull high
GPIO32	SCI_SIO	Output	Pull high
GPIO33	NA	NA	NA
GPIO34	PRSTB#	Output	LPT signal
GPIO35	PRAFD#	Output	LPT signal
GPIO36	PRERR#	Input	LPT signal
GPIO40	TEST_MODE_EN	Input	Pin strap which disabled test mode
GPIO41	PRINT#	Output	LPT signal
GPIO42	LPT_SLIN#	Output	LPT signal
GPIO43	PRACK#	Input	LPT signal
GPIO44	PRBUSY	Input	LPT signal
GPIO45	PRPE	Input	LPT signal

PCH

GPIO	Alt Function	I/O/NC	Power	Tol	Default	Signal Name	Input/Output	Pull-Hi/Pull-Low
GPIO[37]	SATA3GP	I/O	Main	3.3V	GPI	PCH_GPIO37	Input	Pull-Hi
GPIO[38]	SLOAD	I/O	Main	3.3V	GPI	CHASSIS_ID1	Input	Pull-Hi
GPIO[39]	SDATAOUT0	I/O	Main	3.3V	GPI	CHASSIS_ID2	Input	Pull-Hi
GPIO[40]	OC1#	I/O	Resume	3.3V	Native	USB_OC#1	Input	Pull-Hi
GPIO[41]	OC2#	I/O	Resume	3.3V	Native	USB_OC#2	Input	Pull-Hi
GPIO[42]	OC3#	I/O	Resume	3.3V	Native	USB_OC#3	Input	Pull-Hi
GPIO[43]	OC4#	I/O	Resume	3.3V	Native	USB_OC#4	Input	Pull-Hi
GPIO[44]	PCIECLKRQ5#	I/O	Resume	3.3V	Native	PCIECLKREQ5#	Input	Pull-Hi
GPIO[45]	PCIECLKRQ6#	I/O	Resume	3.3V	Native	PCH_GPIO45	Input	Pull-Hi
GPIO[46]	PCIECLKRQ7#	I/O	Resume	3.3V	Native	PCH_GPIO46	Input	Pull-Hi
GPIO[48]	SDATAOUT1	I/O	Main	3.3V	GPI	COM_GPIO1	Input	Pull-Hi
GPIO[49]	SATA5GP	I/O	Main	3.3V	GPI	PCH_GPIO49	Input	Pull-Hi
GPIO[50]	Unmuxed	I/O	Main	3.3V	GPI	FUSB_G1	Input	Pull-Hi
GPIO[51]	Unmuxed	I/O	Main	3.3V	GPO	PCH_GPIO51	Input	NC
GPIO[52]	Unmuxed	I/O	Main	3.3V	GPI	FUSB_G2	Input	Pull-Hi
GPIO[53]	Unmuxed	I/O	Main	3.3V	GPO	PCH_GPIO53	Output	NC
GPIO[54]	Unmuxed	I/O	Main	3.3V	GPI	PCH_GPIO54	Input	Pull-Hi
GPIO[55]	Unmuxed	I/O	Main	3.3V	GPO	PCH_GPIO55	Output	NC
GPIO[57]	Unmuxed	I/O	Resume	3.3V	GPI	PCH_GPIO57	Output	Pull-Hi
GPIO[58]	SML1CLK#	I/O	Resume	3.3V	Native	PCH_SML1CLK	Output	Pull-Hi
GPIO[59]	OC0#	I/O	Resume	3.3V	Native	USB_OC#0	Input	Pull-Hi
GPIO[60]	SML0ALERT#	I/O	Resume	3.3V	Native	PCH_SML0ALERT#	Output	Pull-Hi
GPIO[61]	SUS_STAT#	I/O	Resume	3.3V	Native	SUS_STAT#	Output	NC
GPIO[62]	SUSCLK	I/O	Resume	3.3V	Native	SUS_CLK	Output	NC
GPIO[63]	SLP_S5#	I/O	Resume	3.3V	Native	SLP_S5#	Output	NC
GPIO[64]	CLKOUTFLEX0	I/O	CORE	3.3V	Native	NC	Output	NC
GPIO[65]	CLKOUTFLEX1	I/O	CORE	3.3V	Native	NC	Output	NC
GPIO[66]	CLKOUTFLEX2	I/O	CORE	3.3V	Native	NC	Output	NC
GPIO[67]	CLKOUTFLEX3	I/O	CORE	3.3V	Native	CLKOUTFLEX3_48M	Output	NC
GPIO[68]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO68	Input	Pull-Hi
GPIO[69]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO69	Input	Pull-Low
GPIO[70]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO70	Output	Pull-Low
GPIO[71]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO71	Output	Pull-Hi
GPIO[72]	Unmuxed	I/O	DSW	3.3V	Native	PCH_GPIO72	Output	Pull-Hi
GPIO[73]	PCIECLKRQ0#	I/O	Resume	3.3V	Native	PCH_GPIO73	Input	Pull-Hi
GPIO[74]	SML1ALERT#	I/O	Resume	3.3V	Native	PCH_SML1ALERT#	Output	Pull-Hi
GPIO[75]	SML1DATA	I/O	Resume	3.3V	Native	PCH_SML1DATA	Output	Pull-Hi

SIO(NCT6779D)

PIN NAME	USAGE	Input/Output	NOTES
GPIO46	PRSLCT	Input	LPT signal
GPIO47	RESETCON#	Output	Pull high
GPIO50	SUSWARN#	Input	DSW signal
GPIO51	SIO_5VDUAL	Input	DSW signal
GPIO52	SUSACK#	Output	DSW signal
GPIO53	NA	NA	NA
GPIO54	SLP_SUS#	Input	DSW signal
GPIO55	SYSSVSB_OFF_R	Output	DSW signal
GPIO56	NA	NA	NA
GPIO57	PWR_LED_R	Output	LED drive signal which shows the system state
GPIO60	RND0	I/O	LPT signal
GPIO61	RND1	I/O	LPT signal
GPIO62	RND2	I/O	LPT signal
GPIO63	RND3	I/O	LPT signal
GPIO64	RND4	I/O	LPT signal
GPIO65	RND5	I/O	LPT signal
GPIO66	RND6	I/O	LPT signal
GPIO67	RND7	I/O	LPT signal
GPIO70	DSW_EN	Input	Pin strap which enable DSW
GPIO71	NA	NA	NA
GPIO72	NA	NA	NA
GPIO73	NA	NA	NA
GPIO74	RSTOUT0#	Output	PCIE reset signal
GPIO75	RSTOUT1#	Output	LPC_Debug card reset signal
GPIO76	RSTOUT2#	Output	TPM reset signal
GPIO80	CTSA#	Input	COM port signal
GPIO81	DSRA#	Input	COM port signal
GPIO82	RTSA#	Output	COM port signal
GPIO83	DTRA#	Output	COM port signal
GPIO84	SINA	Input	COM port signal
GPIO85	SOUTA	Output	COM port signal
GPIO86	DCDA#	Input	COM port signal
GPIO87	RIA#	Input	COM port signal

DDR-III DIMM Config

DEVICE	ADDRESS(SA1:SA0)	CLOCK
DIMM 1	00	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 2	10	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1



History

0C-0D change list


- 1. change HDD fan from 3pin no control to 4pin smart fan
- 2. reserve 0402 footprint location next to audio ESD component at all audio line of connector and pin header
- 3. add audio depop schematic for all channel of audio connector and only line out channel of front audio
- 4. connect GPIO57 to PCIE1x pin B12 to control WLAN and GPIO15 to PCIE1x pin A7 to control bluetooth for PCIE1x when wifi card plugged in PCIE1x connector
- 5. SPI_CS0_R# pull high to +VCC3, pull up resistor is 2.2k ohm. Doing this is to give Q83 S an fix voltage level and not let it floating
- 6. remove ALC662VC co-lay schematic
- 7. change LAN connector surge protection from gastube to Sidactor

0D-0E change list

- 1. remove R96 and stuff R178 due to leakage voltage on vcc3
- 2. change R11 to 29.4K, C16 to 470pf, R15 to 21K, C14 to 470pf, R30 to 137K and R79 to 34K for VRM 12.5 transient test solution
- 3. add board ID for NEC H81 bom
- 4. change R486 to 31.6K due to LAN power value is a little high when SA test power ripple noise item
- 5. add 1Kohm resistor to GND on +3VSB_DSW output due to +3VSB_DSW voltage will over spec when system changes from S0 to S5
- 6. change R702 to 33R and C508 to 15pf due to the voltage of CK_PCH_33M_FB is too big
- 7. change R893 to 33R due to the voltage of PCI_CLK0 is too big
- 8. change R690 to 33R due to the voltage of LPC_PCLK is too big
- 9. change low gate damping resistor to 0ohm in every phase due to dead time fail when test VRM power
- 10. change C524 to 180pf due to the voltage of AZ_RST# is a little big
- 11. change R436 to 200K due to 3VSB has a drop when system changes from G3 to S5
- 12. remove external pull up resistor and change C101 to 680pf due to KBRST# will have low pulse when it rises up
- 13. add LEO_CHIP 33M clock
- 14. change C476/C477 to 15pf for more precise 32.678KHz frequency
- 15. EMI solution: change R816/R817/R819/R820 to 300R bead
- 16. EMI solution: add 75R resistor on PWRSW+ trace
- 17. change C295 to 0.1uf and R437 to 100R for ATX_PSON# ring issue when it falls
- 18. mounted VCC5 enable schematic and delay VCC3 enable after VCC5 enable for VR_PG step issue
- 19. mounted L13/L14 for Lenovo EMC request
- 20. add one cap on SATA_LED# for EMC 144MHz harmonic wave issue
- 21. change C254 to 6.8nf, R376 to 14.7K, R370 to 16.2K, EC25 to unstuff to set VCC5 OCP to 35A
- 22. change C43 to 1uf to reduce VCC5 inrush current
- 22. change PCIE standby power to 3VSB as it don't need power at deep S5
- 23. add R875 for PCI wake debug
- 24. add R916 for Lenovo DCL1.8 DDR module new request
- 25. change LAN power source to 3VSB as LAN don't need power in deep s5
- 26. remove 3VA_PCIE schematic as it don't need any more
- 27. change R11 to 30K for lout function and keep R79 value the same with 0C
- 28. add LAN wake switch in page14
- 29. change ME auto recovery schematic for logic error
- 30. change U15/U11/U13/U22/U25/U26 to unstuff; change Q20/Q21/Q22/Q44 PN to D03-7002K69-005
stuff D13/D14 and stuff L10/L12/L15/L16
- 31 U28/U29 can be unmounted if LAN connector has surge protect
- 32 add without LAN surge connector for Malmo and Toulouse
- 33 change DDR external CA/DQ voltage reference component to stuff as internal ref is very unstable
- 34 change R11 to 30.9K/R99 to 75K/R15 to 22.6K to meet intel new lmax 95A

0E-1.0 change list

- 1. add ME auto recovery schematic
- 2. change R134 to 10.7K for power solution
- 3. change R789/R801 to 33R for audio precision test fail
- 4. reserve 1.05V control VR EN schematic
- 5. modify T205/T206 sequence in Reset/Pwrok/PON page
- 6. change fan name to capital
- 7. reserve LAN wake switch schematic as it can wake up the system when system state changes from G3 to S5 with 09A BIOS
- 8. add 1000pf cap on chip_pwrgrd on SIO side for SA test
- 9. add RC delay circuit for DDR switching power. VCC of the chip should be valid earlier than EN
- 10. modify 5VSB contorl schematic as it will have issue from G3 to S5 in without battery condition
- 11.change R102/R103/R117/R118/R127/R128/R139/R140 to 10K to reduce draw current
- 12. change R722/R721 to 10Kohm
- 13. change EC11 to unstuff, EC10 to stuff for maunfactory
- 14. change XDP part to reserve, stuff R808



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